

# Iris 14"/15" Schematics

## Bay Trail - M

2014-11-11

REV : A00

*DY : None Installed*

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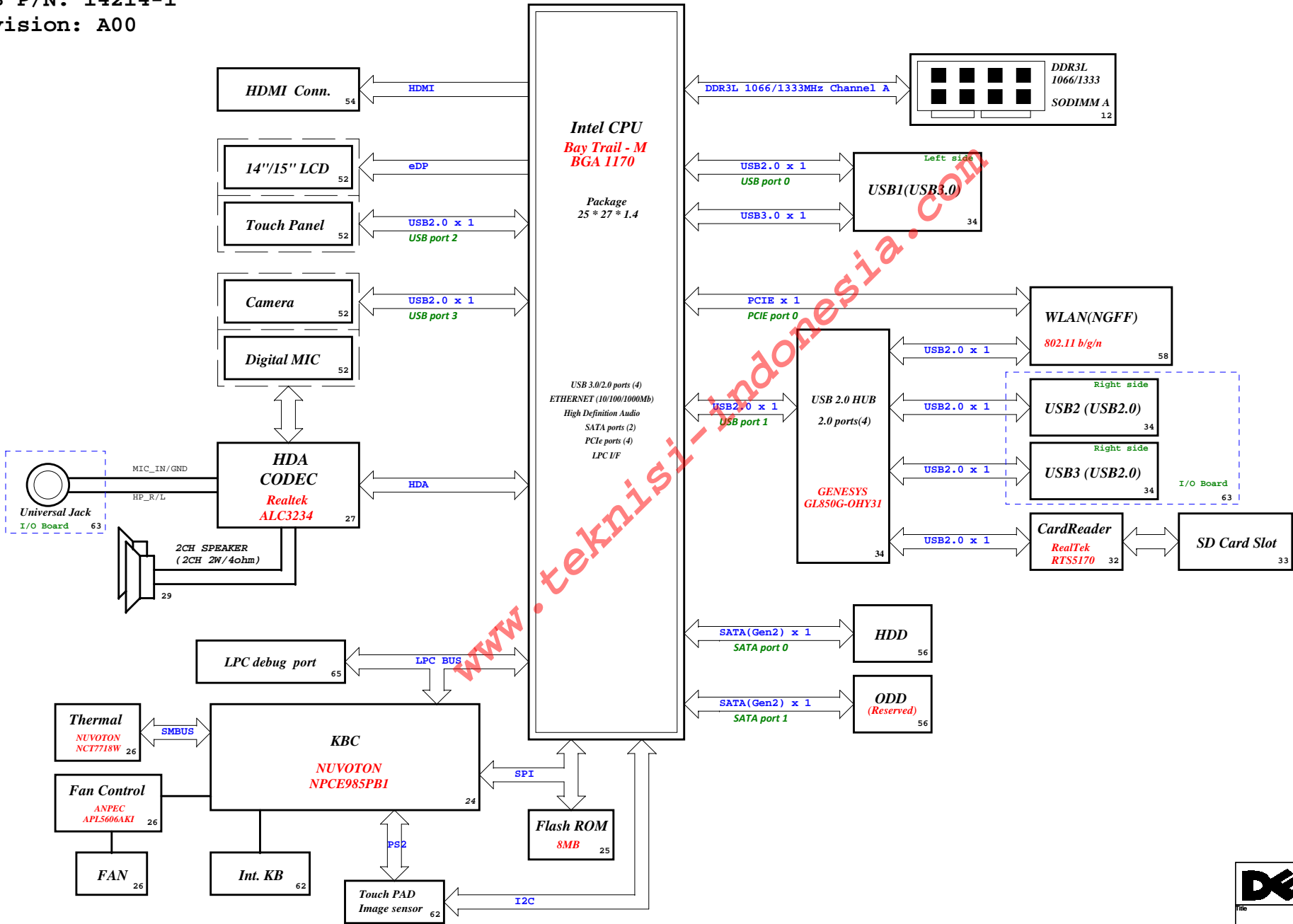
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<b>Cover Page</b>		
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Project code:  
4PD02V010001 (14")  
4PD030010001 (15")

PCB P/N: 14214-1  
Revision: A00

# Iris Bay Trail-M Block Diagram



CHARGER	
BQ24727RGR-1-GP 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT
SYSTEM DC/DC	
TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95833HRTZ-GP 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0
CPU 1.05V	
SY8206DQNC-GP-U 50	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
CPU 1.0V	
RT9041E-12GQW-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D0V_S5
System LDO 1.8V	
S-1339D18-M5T1U3-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
System LDO 1.5V	
S-1339D15-M5001-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
System switches	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D8V_S5	1D8V_S0
1D35V_S3	1D35V_S0
PCB LAYER	
L1:Top L2:GND L3:Signal L4:Signal L5:VCC L6:Bottom	


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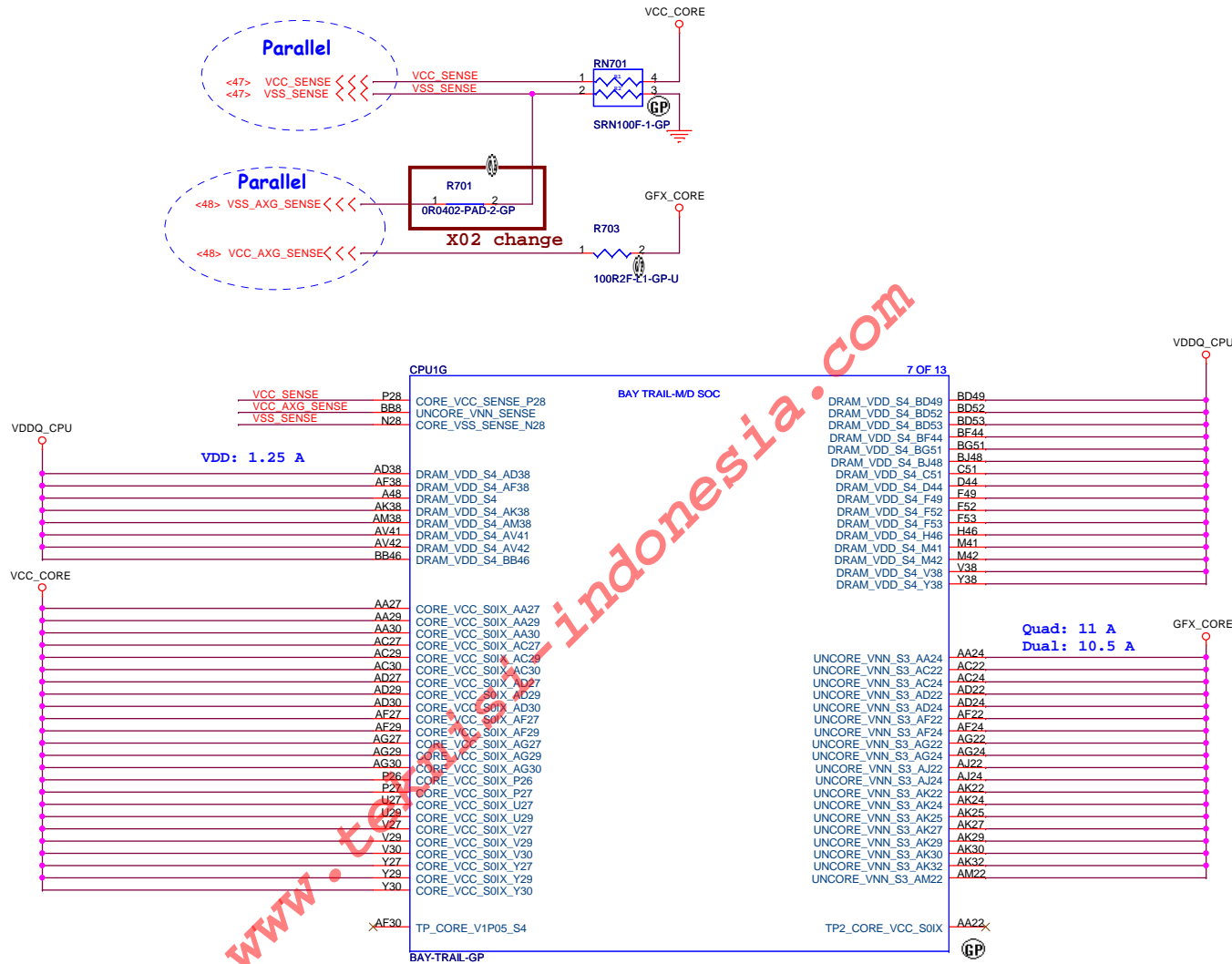
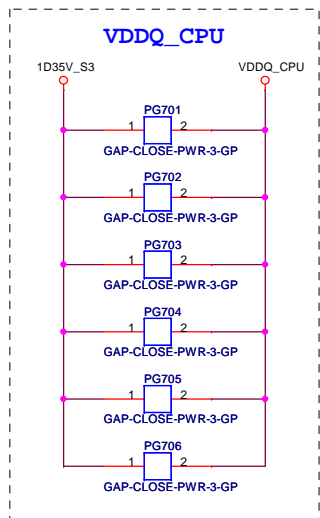
# Blanking

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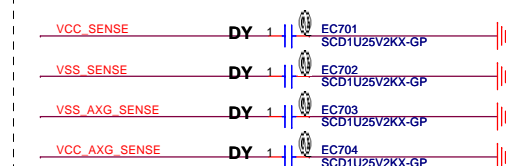
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### EMI Caps.



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DDI0\_DDCDATA(C26): Strap Pin for DDI0 Detect  
DDI0\_DDCDATA = 1 DDI0 detected  
DDI0\_DDCDATA = 0 DDI0 not detected

LCD

DDI1\_DDCDATA(P30): Strap Pin for DDI1 Detect  
DDI1\_DDCDATA = 1 DDI1 detected  
DDI1\_DDCDATA = 0 DDI1 not detected

PORT	DDI Pin Names	DisplayPort* Mapping	HDMI Mapping
PORT-0	DDI0_TXP[0]	DP0_MAINP[0]	TMD50_DATAP[2]
	DDI0_TXN[0]	DP0_MAINN[0]	TMD50_DATAN[2]
	DDI0_TXP[1]	DP0_MAINP[1]	TMD50_DATAP[1]
	DDI0_TXN[1]	DP0_MAINN[1]	TMD50_DATAN[1]
	DDI0_TXP[2]	DP0_MAINP[2]	TMD50_DATAP[0]
	DDI0_TXN[2]	DP0_MAINN[2]	TMD50_DATAN[0]
	DDI0_TXP[3]	DP0_MAINP[3]	TMD50_CLKP
	DDI0_TXN[3]	DP0_MAINN[3]	TMD50_CLKN
	DDI0_AUXP	DP0_AUXP	NA
	DDI0_AUXN	DP0_AUXN	NA
	DDI0_HPDP	DP0_HPDP	TMD50_HPDP
	DDI0_DDCCCLK	NA	TMD50_DDCCCLK
	DDI0_DDCDATA	DP0_EN	TMD50_DDCDATA
	DDI0_VDDEN	EDP0_VDDEN	NA
	DDI0_BKLCTEN	EDP0_BKLCTEN	NA
	DDI0_BKLCTL	EDP0_BKLCTL	NA
	DDI1_RCOMP_P	NA	NA
	DDI1_RCOMP_N	NA	NA

<15> GPIO\_S0\_NC13 >>>

TP801 1 GPIO\_S0\_NC13  
TPAD14-OP-GP 1 GPIO\_S0\_NC14 C29  
TP801 1 GPIO\_S0\_NC12  
TPAD14-OP-GP 1 GPIO\_S0\_NC12



BAY-TRAIL-GP

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CPU (DDI/EDP/GPIO)

Size A3

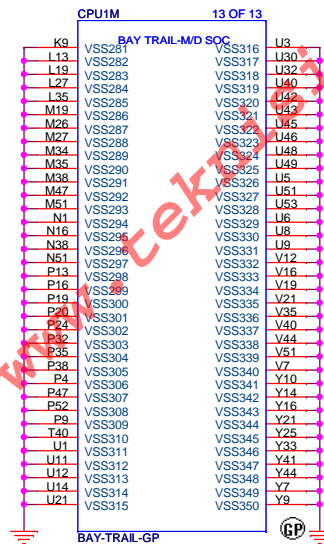
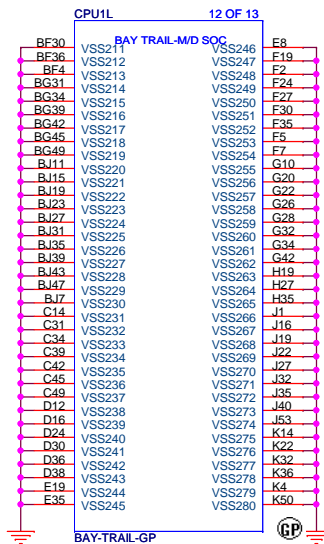
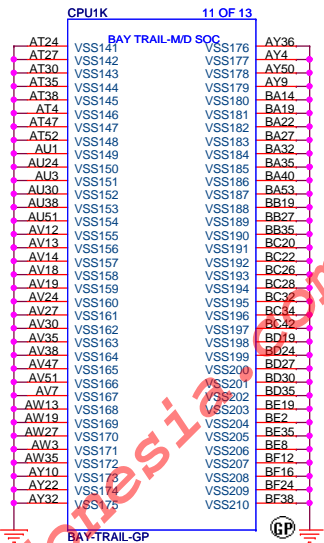
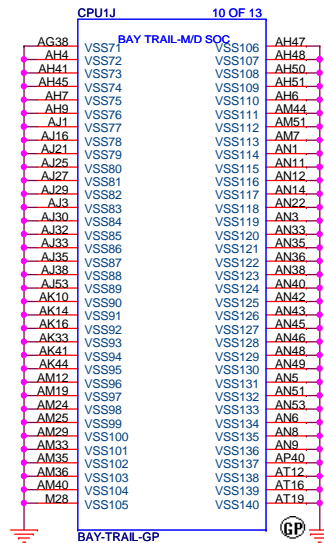
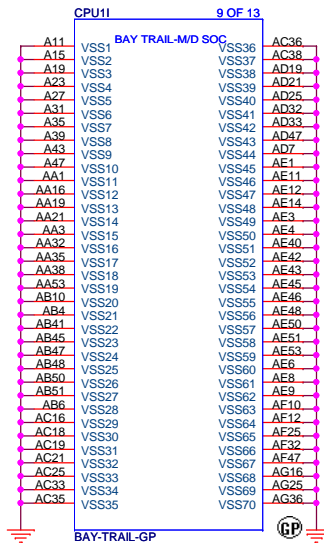
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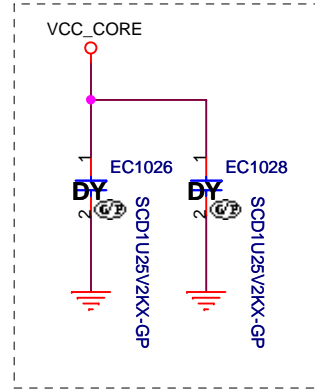
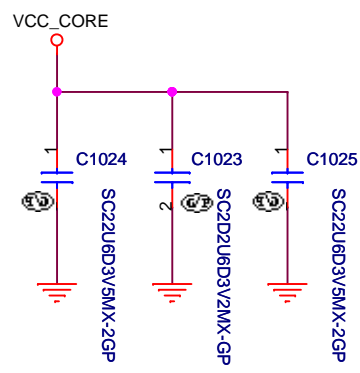
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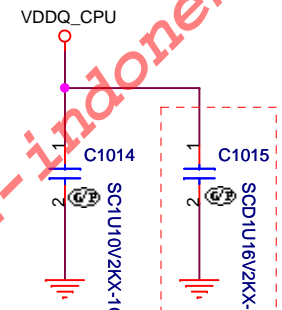
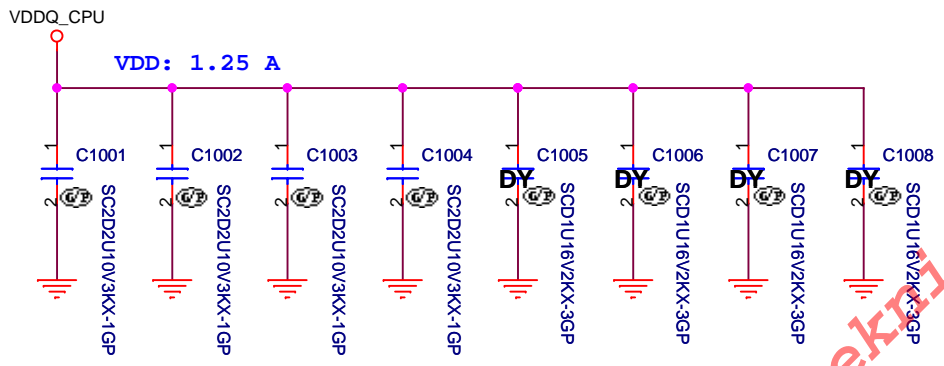
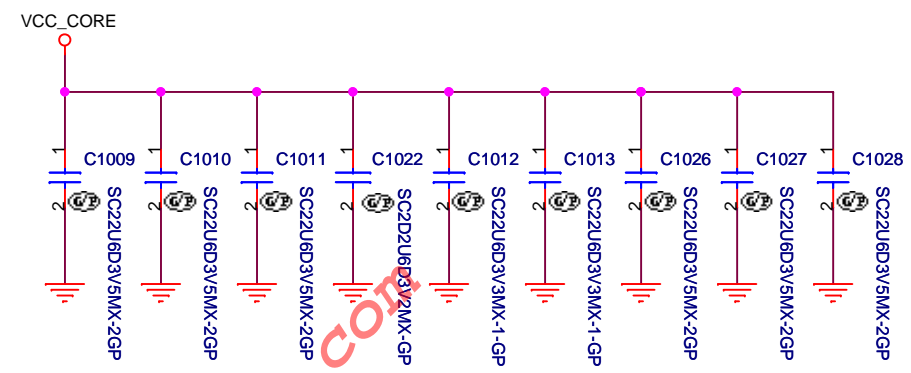


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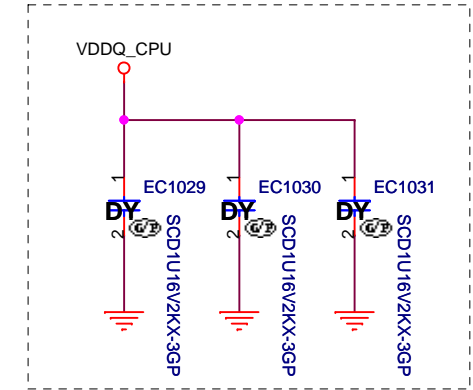
Main Func = CPU



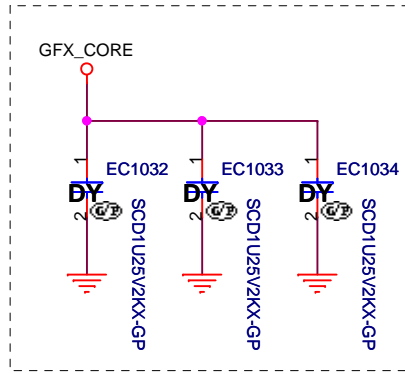
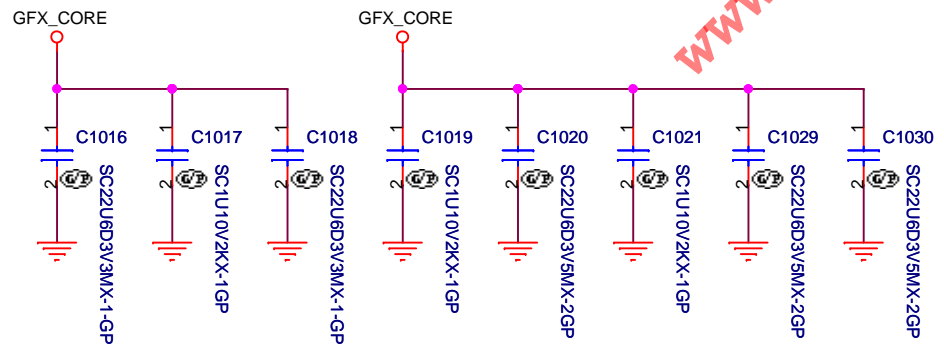
EMI Caps.



close to pin AD38 & AF38




EMI Caps.



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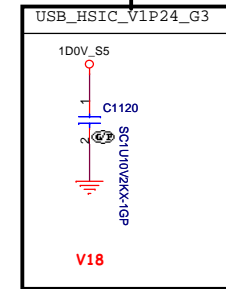
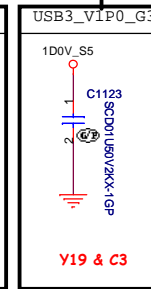
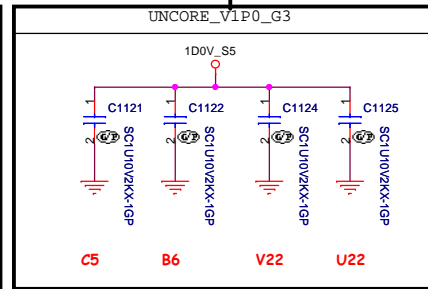
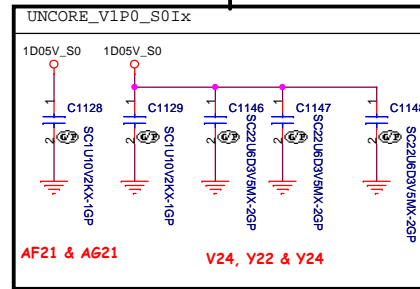
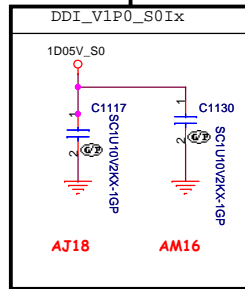
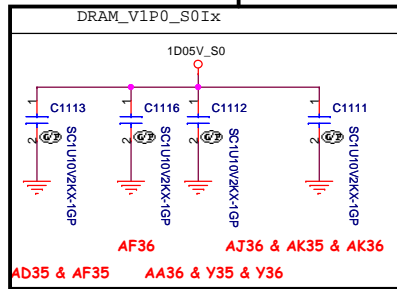
Title <b>CPU (Power CAP1)</b>		
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VLP0Sx: 2.1 A

VLP0A: 0.35 A

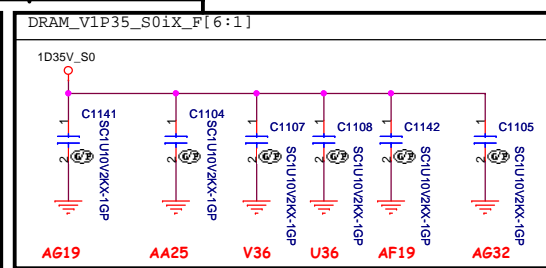
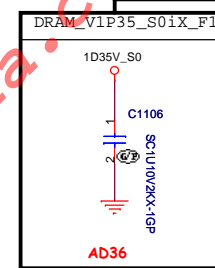
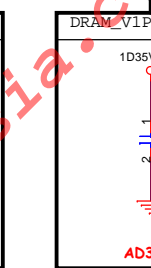
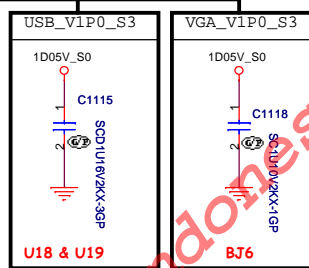
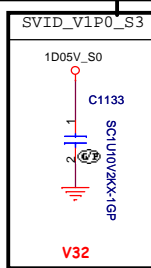
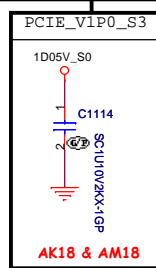
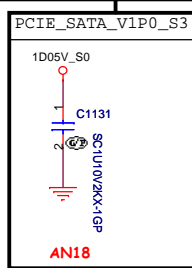
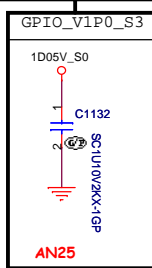
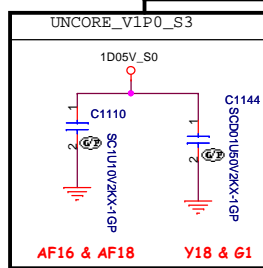
VLP24A: 0.035 A



V18: USB\_HSIC\_VLP24\_G3 pin(s) can be connected to VLP0A platform rail if USB HSIC is not used.

VLP0S: 0.9 A

VLP35Sx (VSFR): 0.4 A

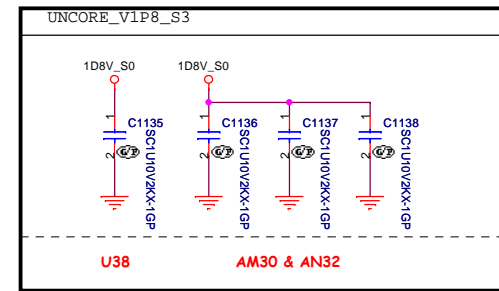
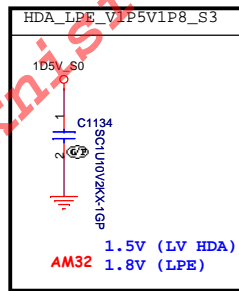
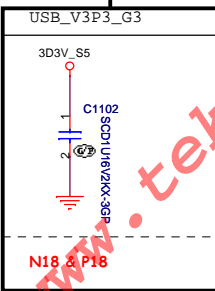
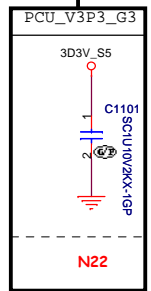
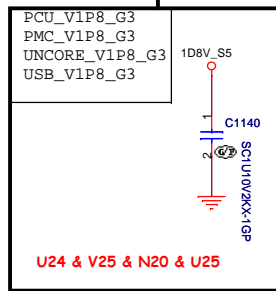
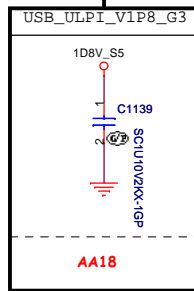


VLP8A: 0.065 A

V3P3A: 0.055 A

VLP5VLP8S (VAUD):  
See VLP8S

VLP8S: 0.01 A

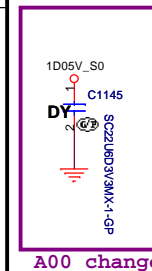
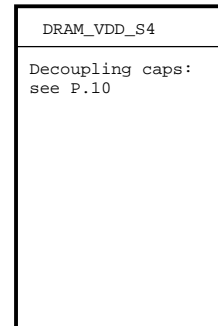
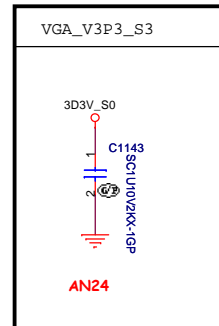
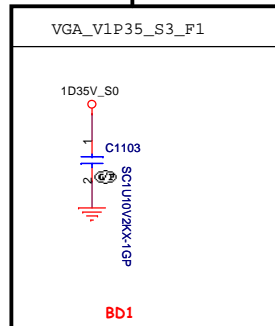
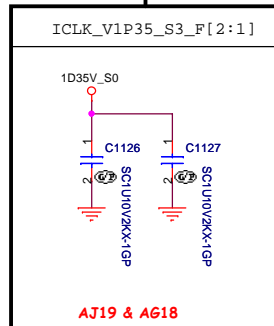
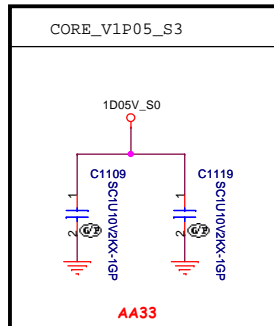


VLP0S5: 1.1 A

VLP35S: 0.045 A

V3P3S: 0.03 A

VDD: 1.25 A



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STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

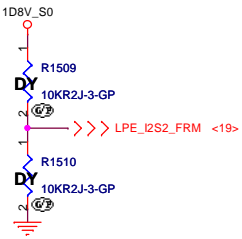
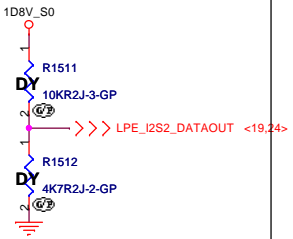
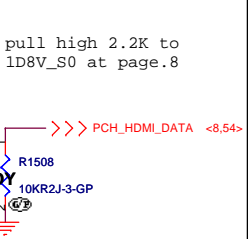
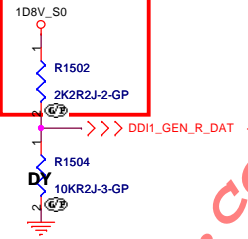
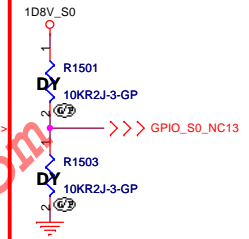
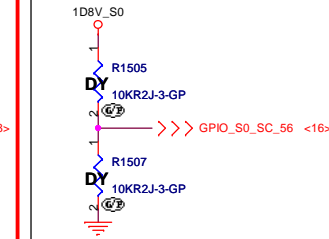
Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap (A16 Override)
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI (Default)	Normal Operation (Default)	DDI0 detected	DDI1 detected	DDI1 detected	Top address bit is unchanged (Default)
Low	LPC	Override	DDI0 not detected (Default)	DDI1 not detected (Default)	DDI1 not detected	Top address bit is inverted

Table 20. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is inverted 1 = Top address bit is unchanged
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

INTEL BTM EDS Rev2.5

## 30.2 LPE\_I2S2\_DATAOUT/ GPIO\_S0\_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO\_S0\_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

### 27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

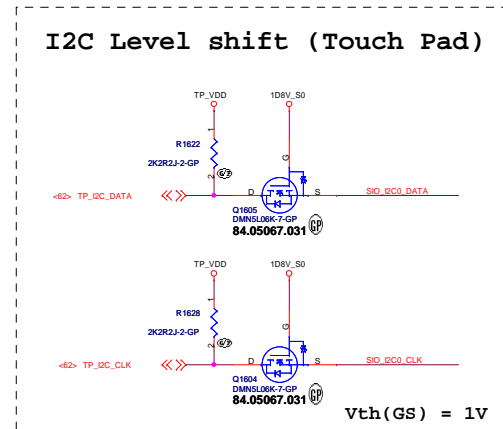
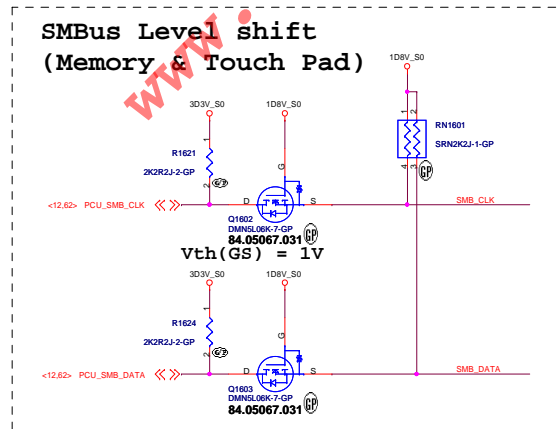
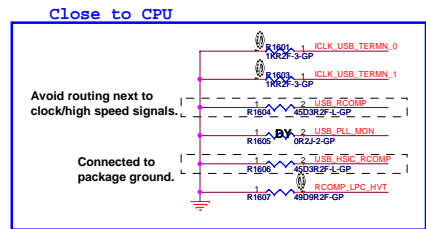
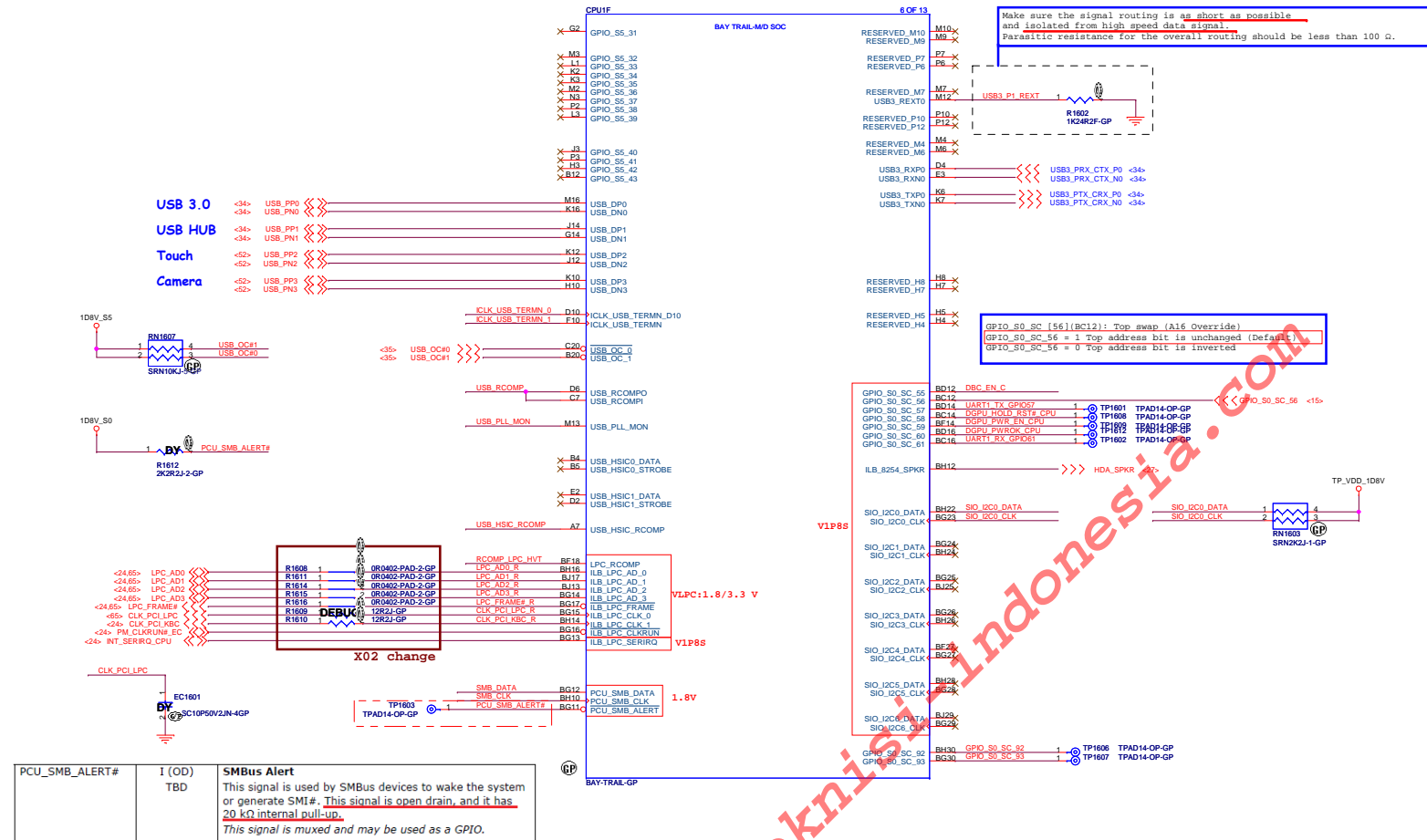
**Note:** The Top-Swap strap is an active high signal and is multiplexed with the GPIO\_S0\_SC[56] signal.

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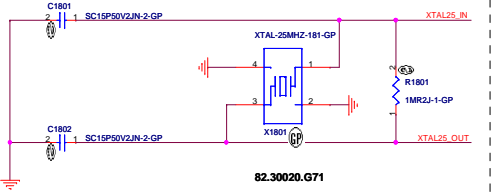
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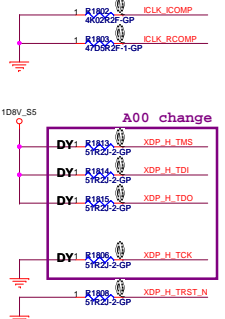
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
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Main Func = PCH

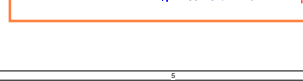
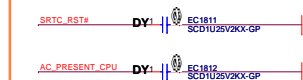
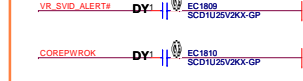
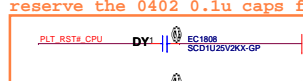
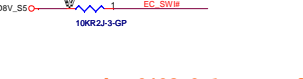
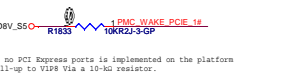
Crystal: 25 MHz



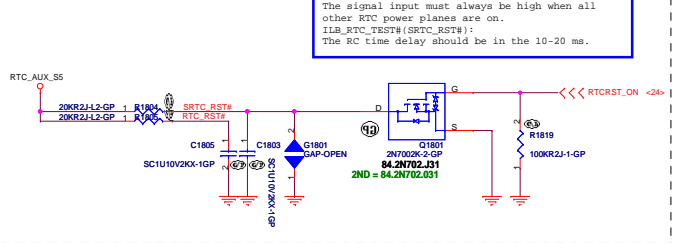
EE Note:  
C1801 and C1802:  
Select the capacitance base on the crystal measurement result.



(CRB#509728)  
Layout Note:  
1. PLACE R1806, R1813, R1814 WITHIN 1.1" FROM SOC PIN  
2. PLACE R1815 WITHIN 0.25" FROM XDP PIN

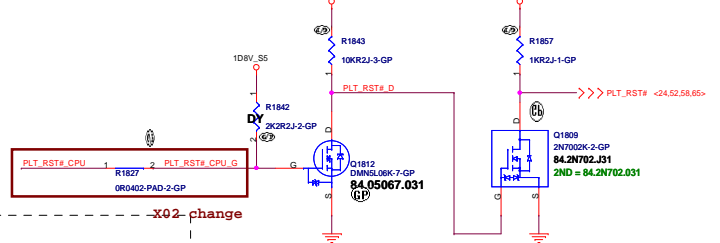


RTC Reset

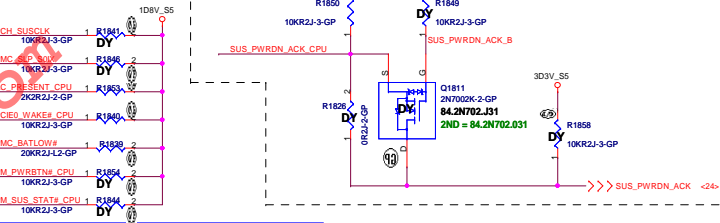


ILB\_RTC\_RST#(RTC\_RST#):  
The signal input must always be high when all other RTC power planes are on.  
ILB\_RTC\_TESTH(SRTC\_RST#):  
The RC time delay should be in the 10-20 ms.

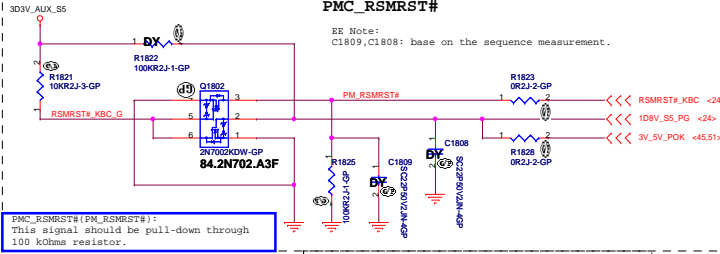
Level shift



EE Note:  
R1857: base on the Measurement of PL7\_RST#.



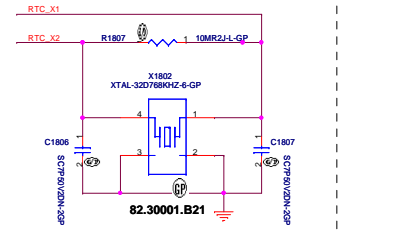
PM\_PRESBTA\_CPU (PM\_PRESBTA#):  
This signal has an internal pull-up resistor and has an internal ~16 ms de-bounce on the input.



EE Note:  
C1809, C1808: base on the sequence measurement.

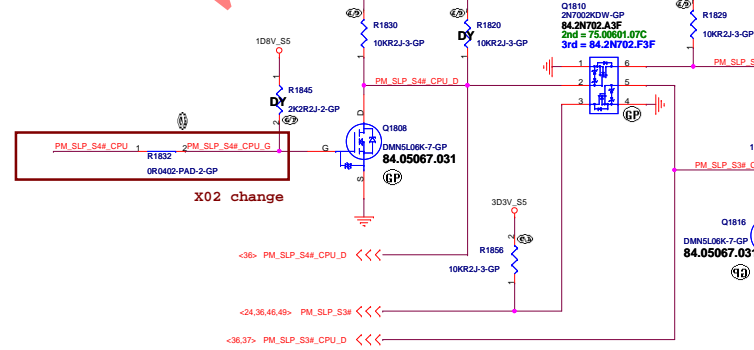
PM\_RSMRST#(PM\_RSMRST#):  
This signal should be pull-down through 100 kohms resistor.

Crystal: 32.768 kHz



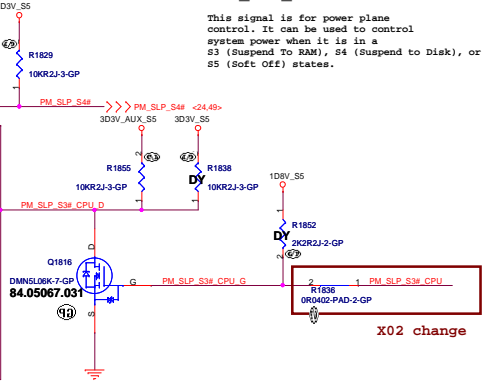
PMC\_SLP\_S4#

This signal is for power plane control. It can be used to control system power when it is in a S4 (Suspend to Disk) or S5 (Soft Off) state.

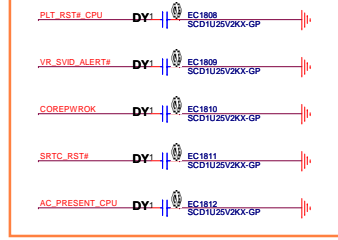


PMC\_SLP\_S3#

This signal is for power plane control. It can be used to control system power when it is in a S3 (Suspend to RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.



reserve the 0402 0.1u caps for EMI



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# Main Func = PCH

SATA\_GP:  
When used as an interlock switch status indication, this signal should be driven to '0' to indicate that the switch is closed, and to '1' to indicate that the switch is open.

HDD

ODD

WLAN

V1P8S

VAUD

V1P8S

VAUD

V1P8S

VAUD

V1P8S

VAUD

V1P8S

VAUD

V1P8S

VAUD

V1P8S

VAUD

V1P8S

VAUD

V1P8S

VAUD

Figure 96. Root Port Configuration Options

(4) x1				(1) x2, (2) x1			
PCIe* 2.0				PCIe* 2.0			
RP 1	RP 2	RP 3	RP 4	Root Port 1	RP 2	RP 3	
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 2	Lane 3
(1) x4				(2) x2			
PCIe* 2.0				PCIe* 2.0			
Root Port 1				Root Port 2			
Lane 0				Lane 0			
Lane 1				Lane 1			
Lane 2				Lane 2			
Lane 3				Lane 3			

Root port configurations are set by SoftStraps stored in SPI flash, and the default option is "(4) x1". Links for each root port will train automatically to the maximum possible for each port.

Terminating unused PCI Express ports  
If a PCI Express port is not implemented on the platform, the PCIE\_TXP/N [x] and PCIE\_RXP/N [x] signals of that port can be left as No-connect.

X02 change

VAUD:  
1.5 V rail for HD Audio.  
1.8 V rail for I2S. on in S0 only.

SATA\_DEVSLP (AY14,BA24,BF28): V1P8S  
SATA\_DEVSLP = 1, SATA\_DEVSLP requests the SATA device to enter into the DEVSLP power state.  
SATA\_DEVSLP = 0, SATA\_DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

GPIO\_S0\_SC[063] (BA30): Strap Pin for BIOS Boot Selection  
LPE\_I2S2\_FRM = 1 SPI  
LPE\_I2S2\_FRM = 0 LPC  
GPIO\_S0\_SC[065] (BC30): Strap Pin for Security Flash Descriptors  
LPE\_I2S2\_DATAOUT = 1 Normal Operation  
LPE\_I2S2\_DATAOUT = 0 Override

Intel CHERST V2.0 (#509653)  
70.7 Ω ±5% (67.165 Ω-74.235 Ω) pull-up to V1P08

H\_PROCHOT# <24,44,46>

HDA CODEC\_BITCLK <27>  
HDA CODEC\_RST# <27,29>

HDA SYNC <27>  
HDA SYNC\_R <27>

HDA CODEC\_SYNC <27>

HDA RST#

HDA SYNC

HDA SYNC\_R

HDA CODEC\_SYNC

HDA RST#

HDA SYNC


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Main Func = PCH

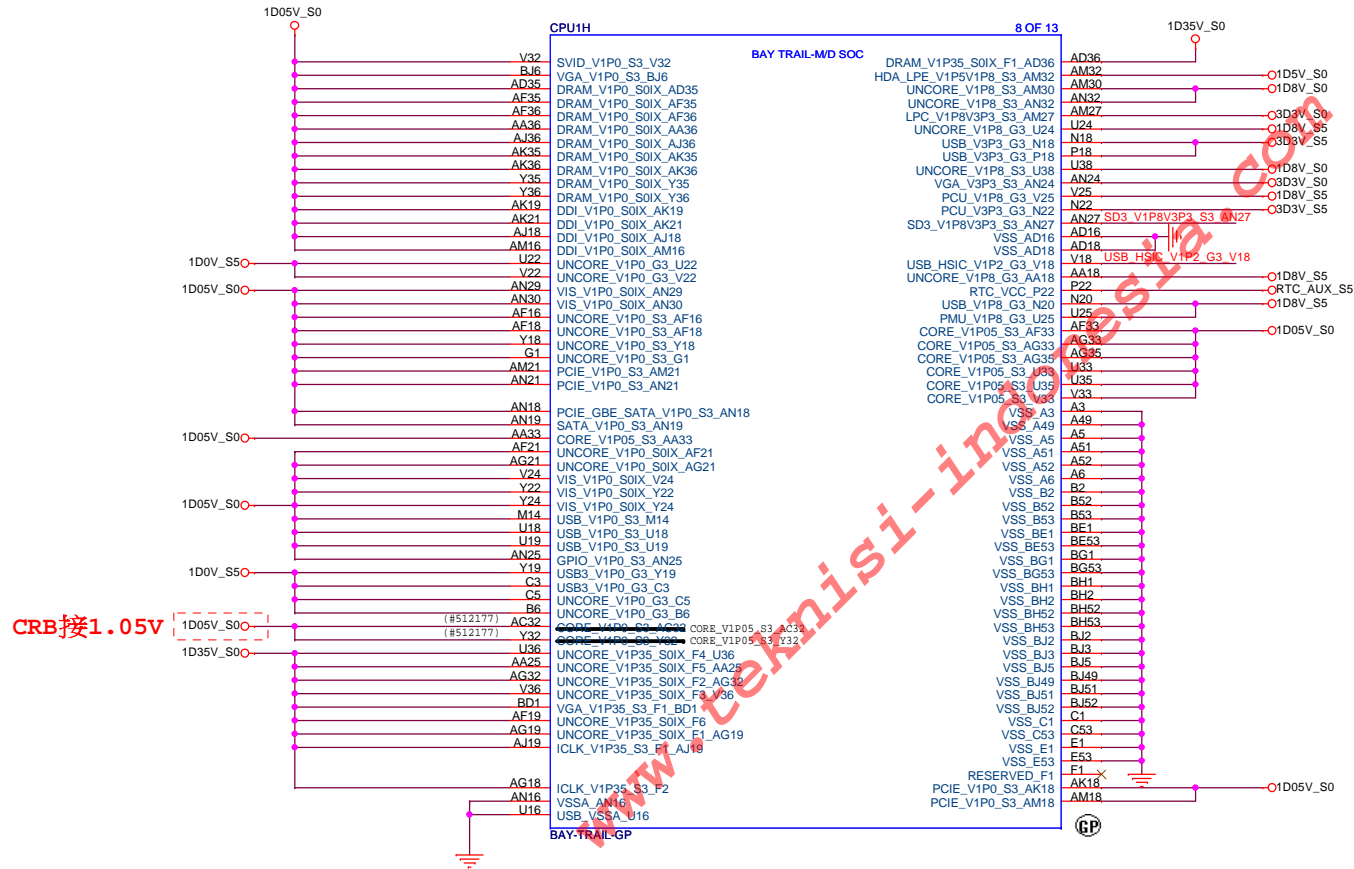
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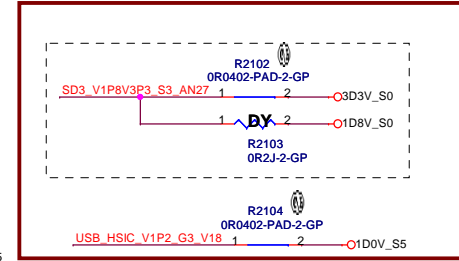
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Main Func = PCH



X02 change



(#512177/EDS)  
V18: USB\_HSIC\_V1P24\_G3 pin(s) can be connected to V1P0A platform rail if USB HSIC is not used.


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Main Func = PCH

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Main Func = PCH

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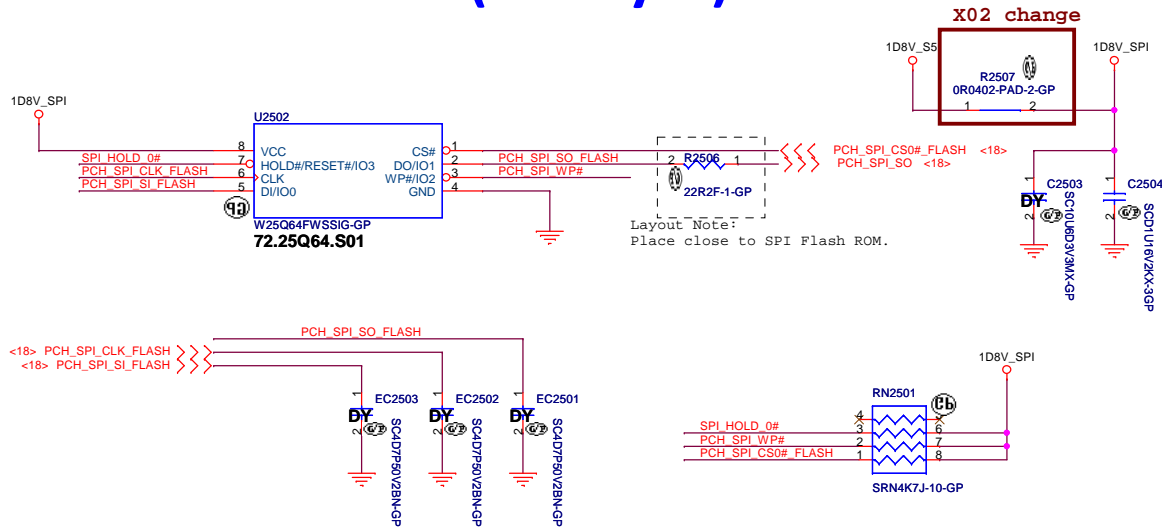
1





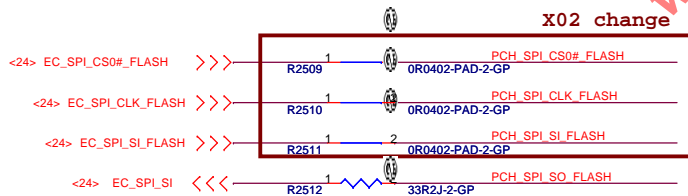
Main Func = SPI Flash

## SPI FLASH ROM (8M byte) for CPU



X02 change

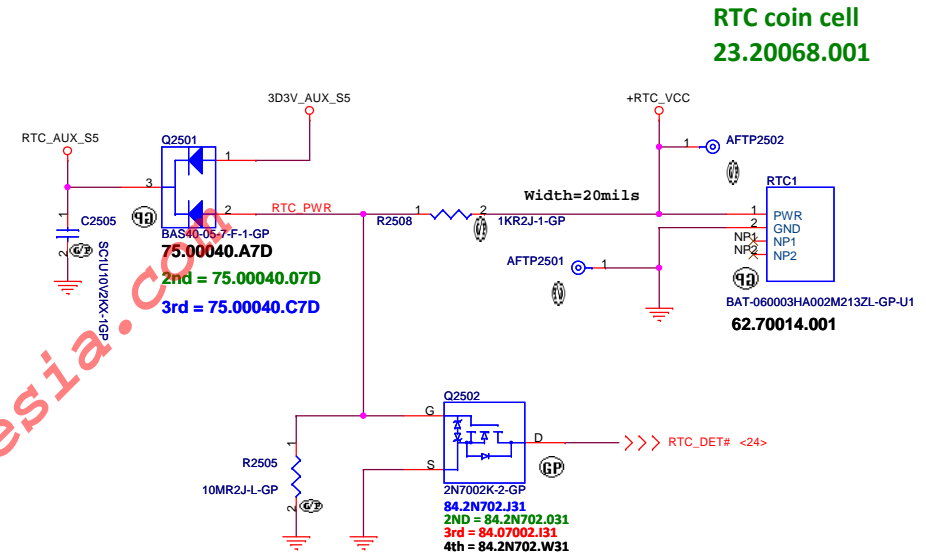
## SPI ROM link to KBC



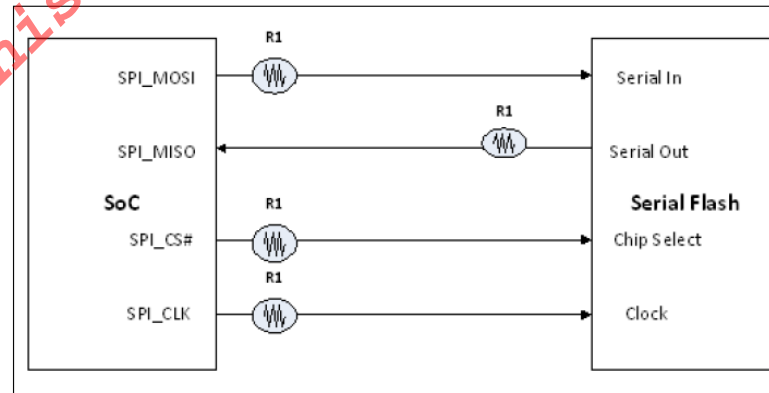
X02 change

Main Func = RTC

## RTC Battery



RTC coin cell  
23.20068.001



### NOTES:

1. R1 = 22  $\Omega$  should be placed close to the SoC for SPI\_MOSI, SPI\_MISO and SPI\_CLK signals.
2. R1 = 22  $\Omega$  should be placed close to the Serial Flash IC for SPI\_MISO signal

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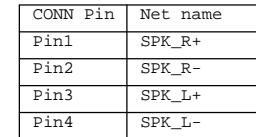
# Blanking

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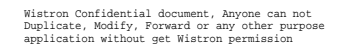
# Speaker

Speaker trace\_width >40mil @ 2w4ohm speaker power



x01 change

Audio jack on I/O Board.




Main Func = LAN

Blanking

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Main Func = LAN

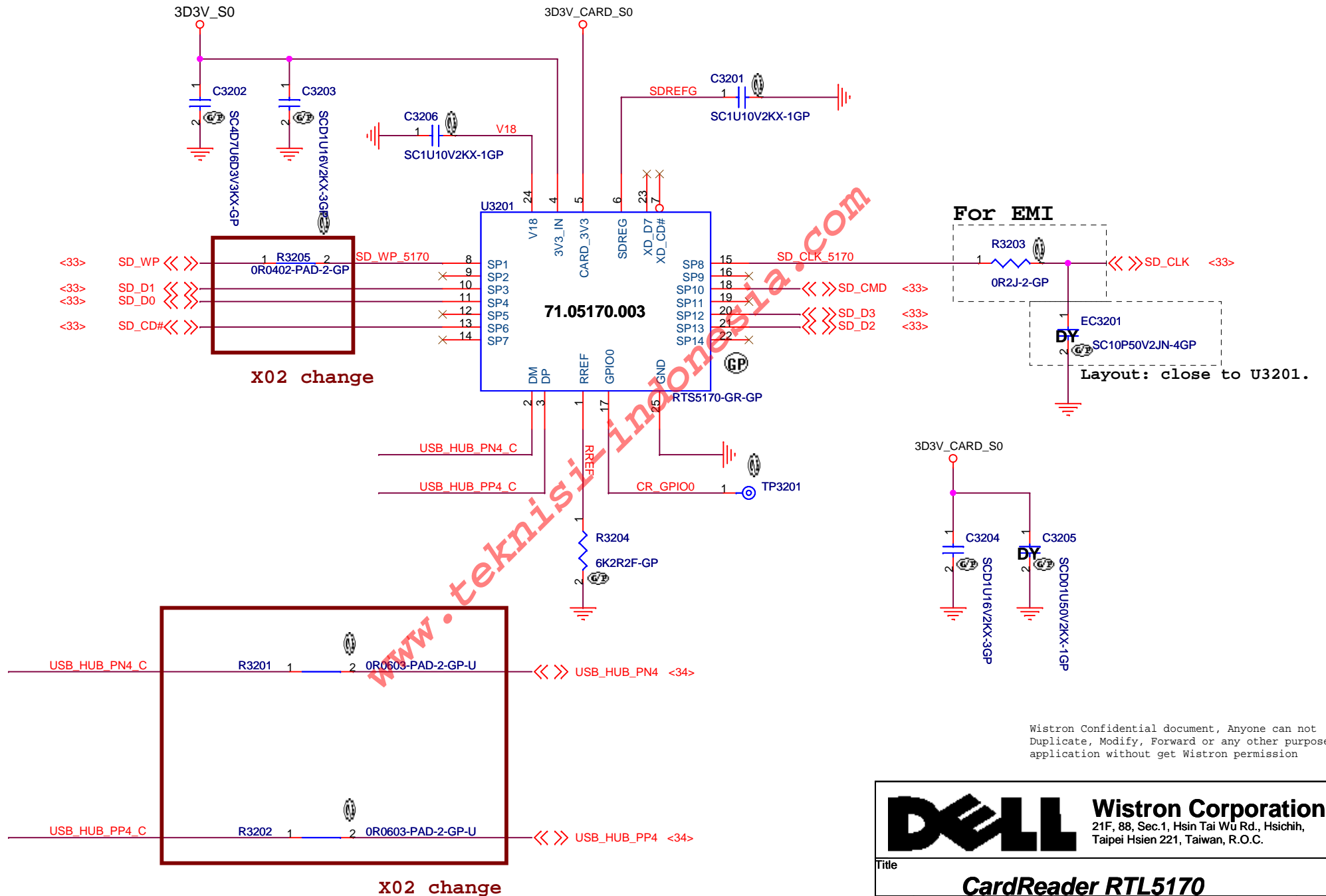
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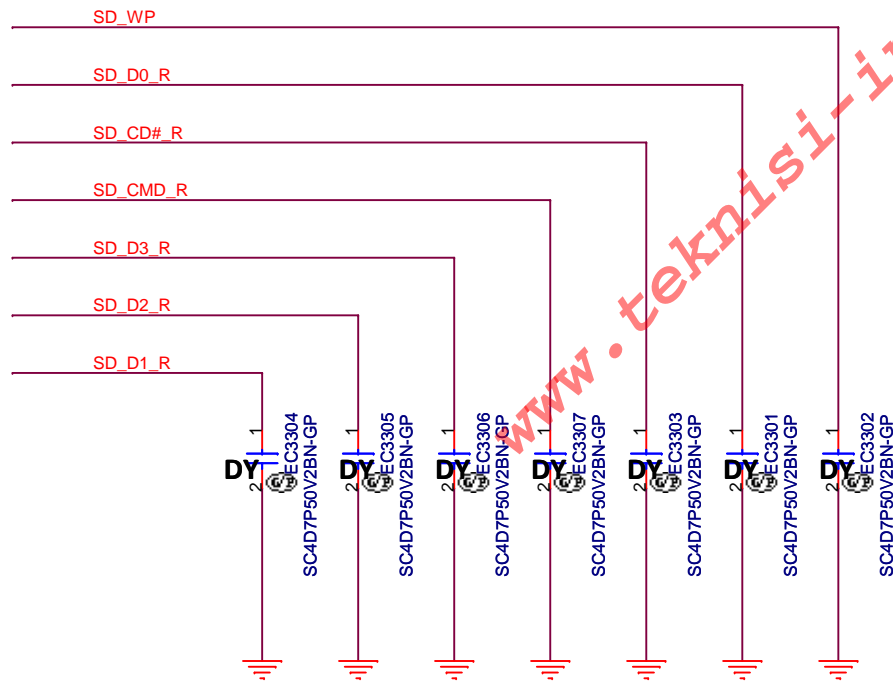
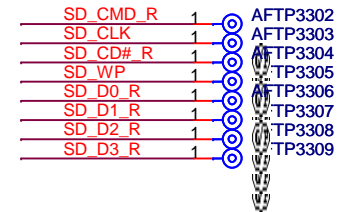
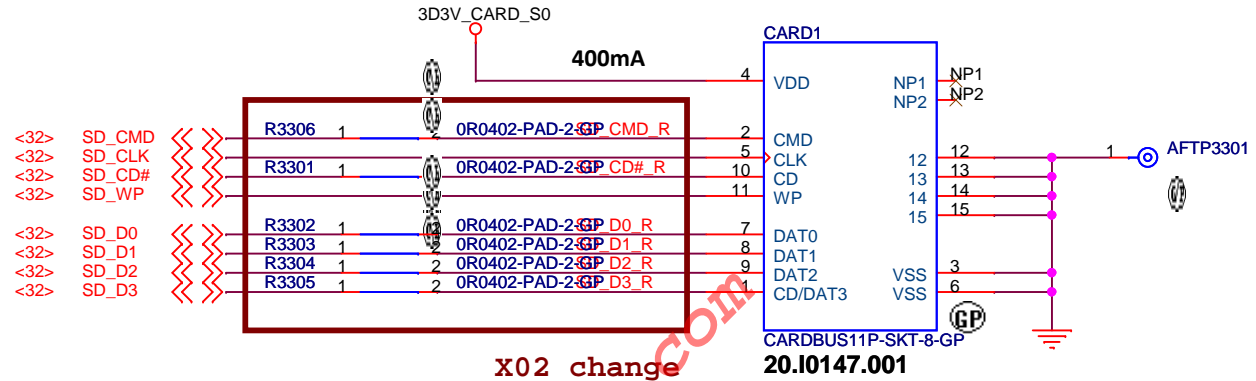
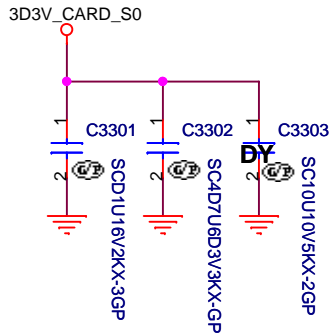
# Main Func = Card Reader



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		<b>CardReader RTL5170</b> <b>Iris BTM</b>	
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**Main Func = Card Reader**



Without card	
Inserted card(lock)	
Inserted card(unlock)	

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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

### **Card Reader CONN**

Size  
A4

Document Number

## Iris BTM

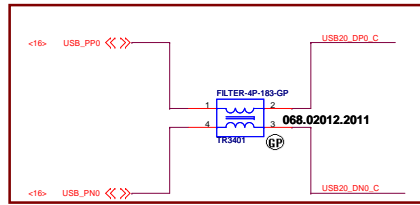
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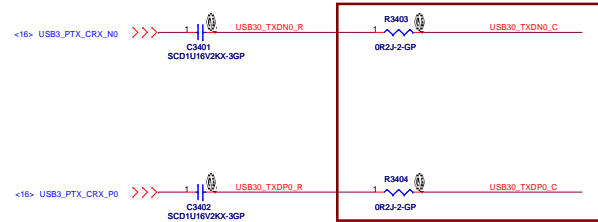
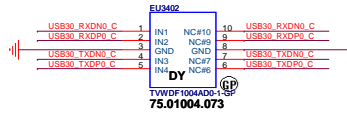
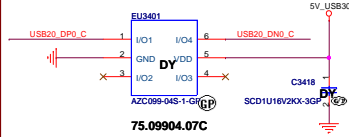
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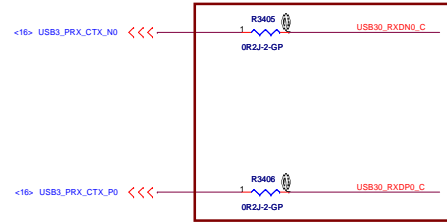
## Main Func = USB3.0 Port1



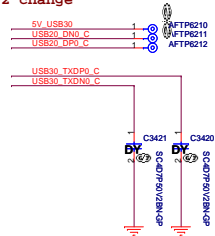
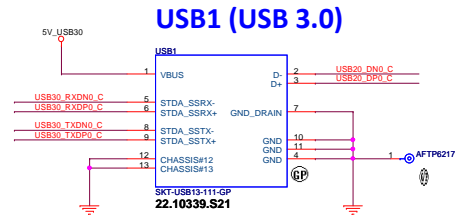
X02 change



X02 change



X02 change



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

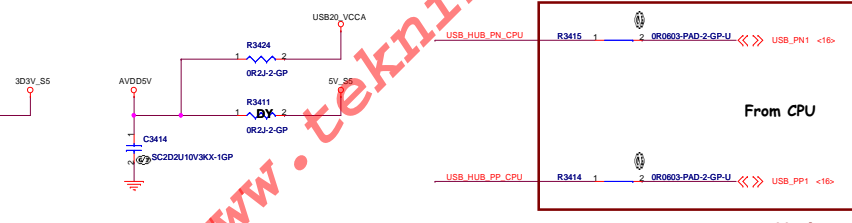
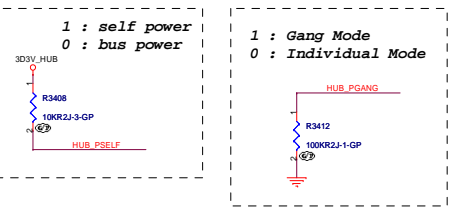
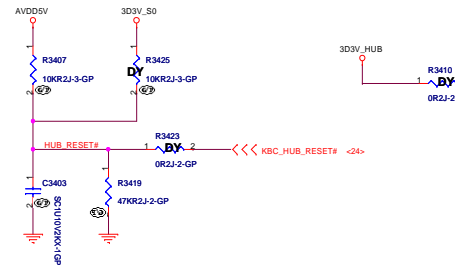
## Main Func = USB2.0 Port2

USB connector on I/O Board.

## Main Func = USB2.0 Port3

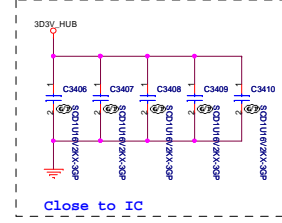
USB connector on I/O Board.

## Main Func = USB Hub

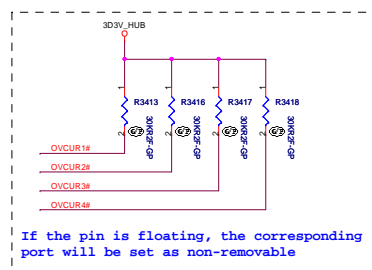


From CPU

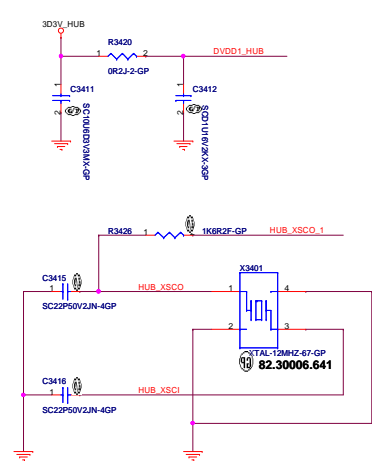
X02 change



Close to IC

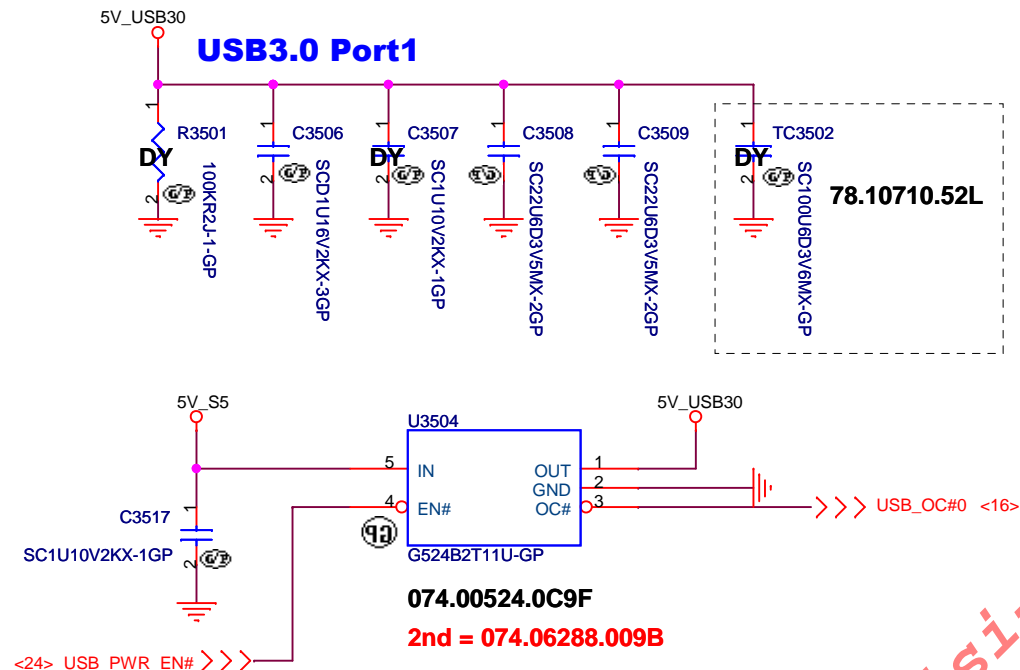


If the pin is floating, the corresponding port will be set as non-removable

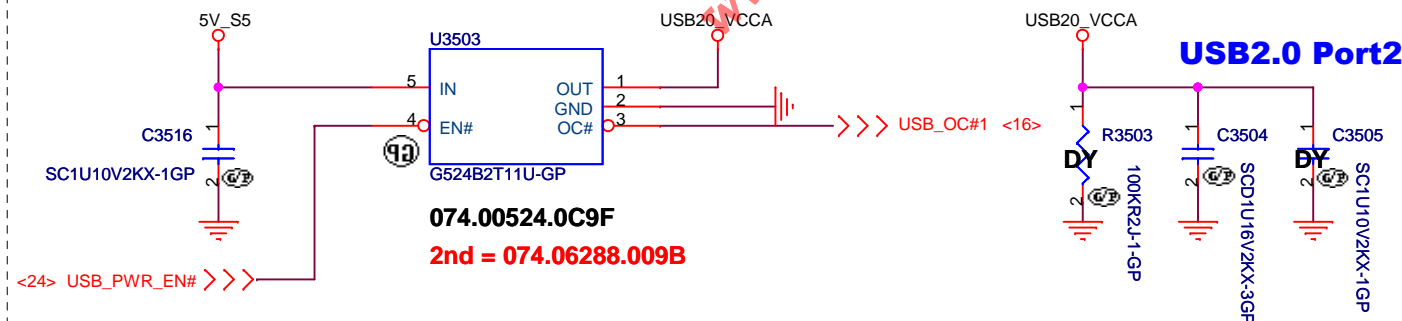


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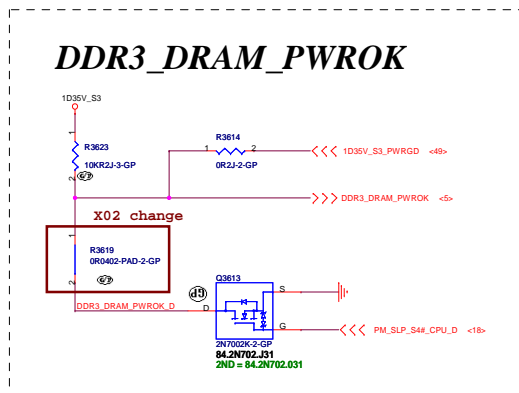
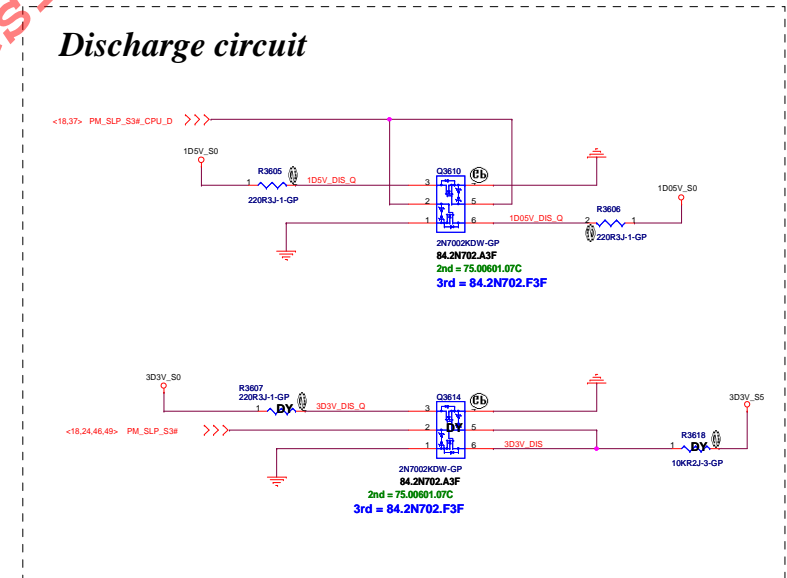
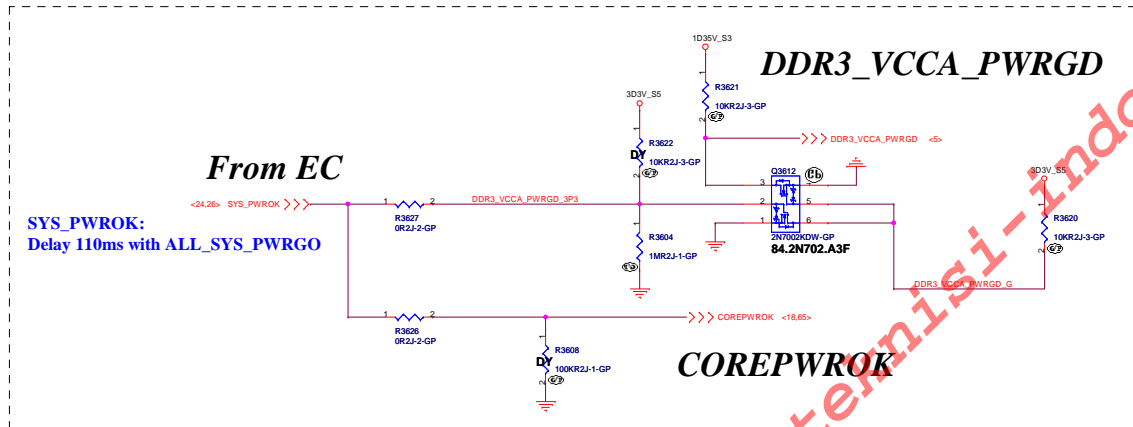
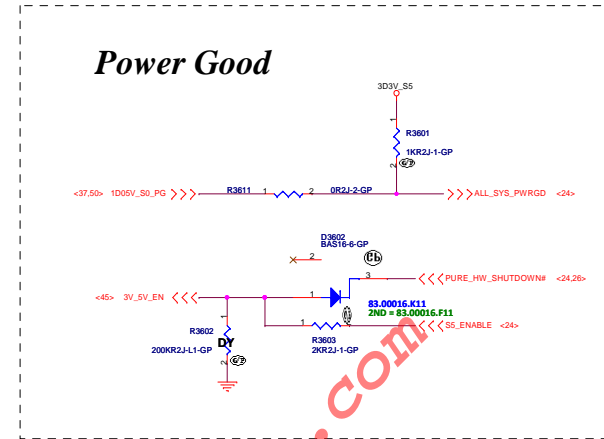
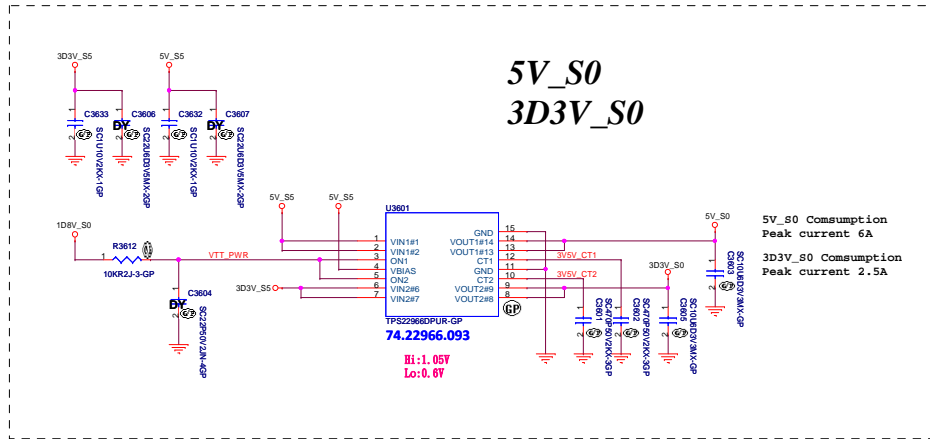
## Main Func = USB3.0



## Main Func = USB2.0

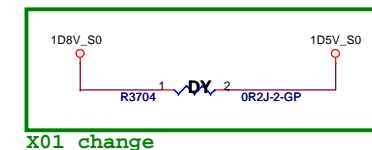
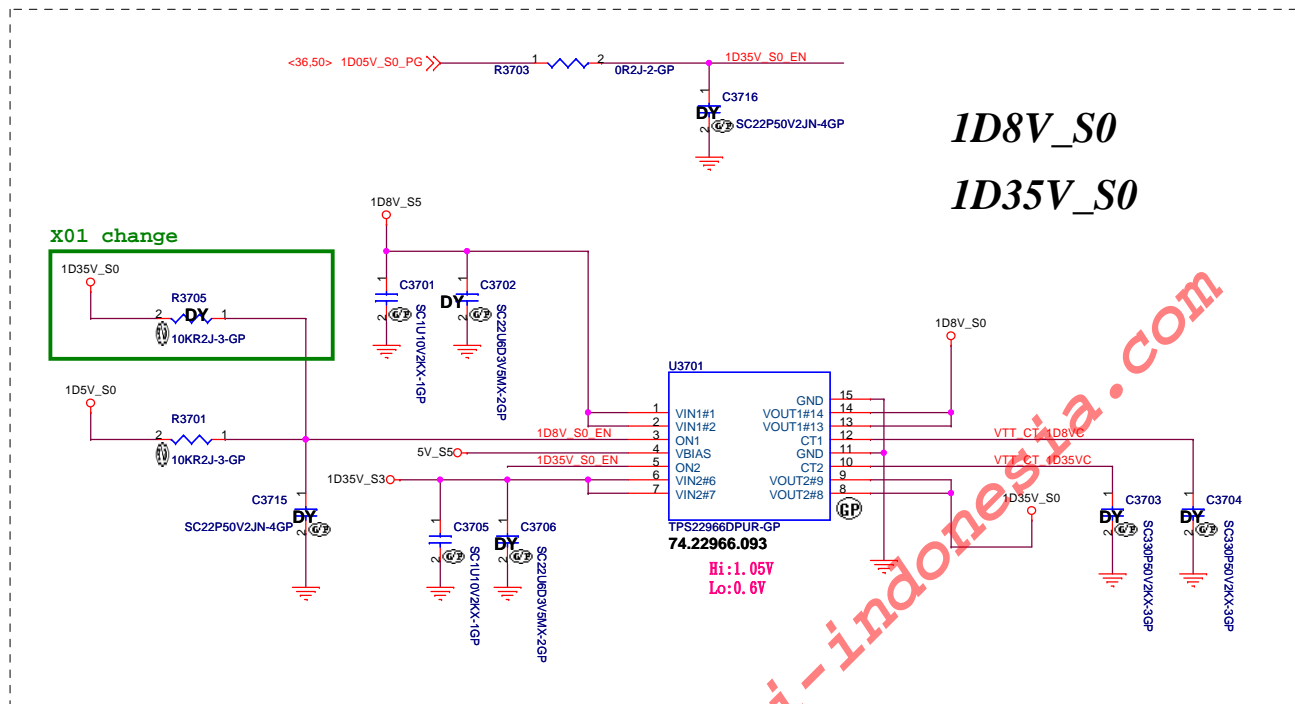


# Main Func = Power Plane & Sequence

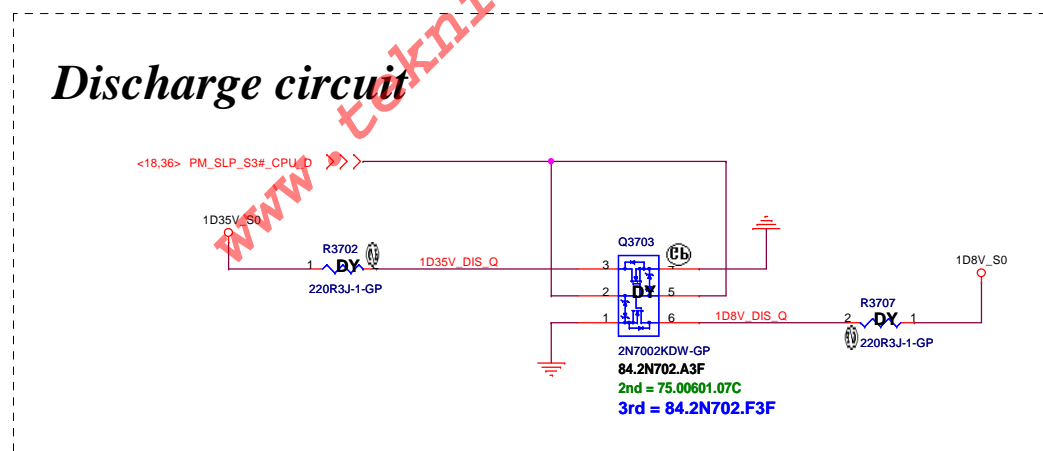


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# Main Func = Power Plane & Sequence



## Discharge circuit



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Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
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Document Number  
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Rev  
**A00**


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Size  
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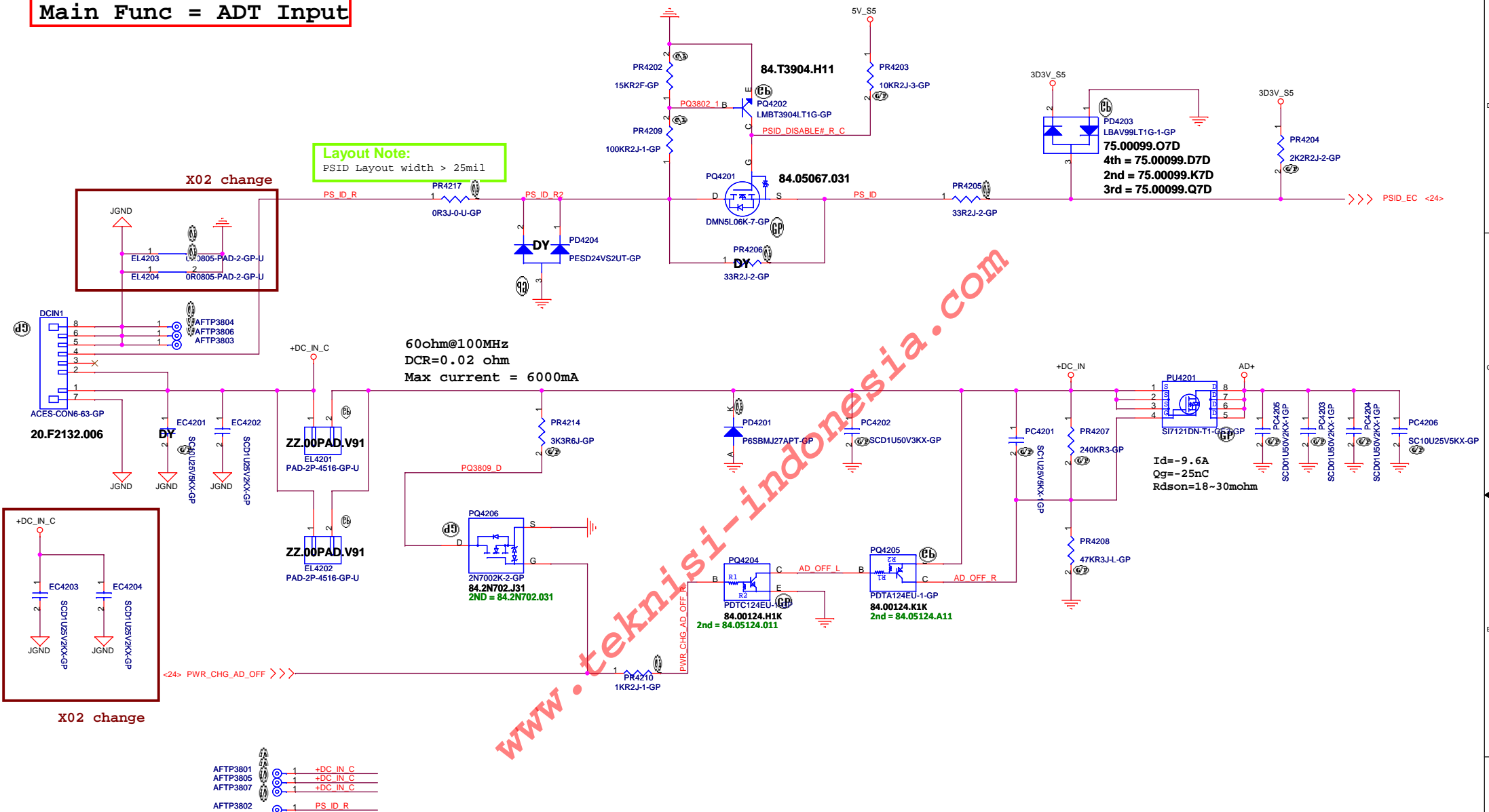
Document Number  
**Iris BTM**

Rev  
**A00**

Date: Tuesday, November 11, 2014

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**Main Func = ADT Input**

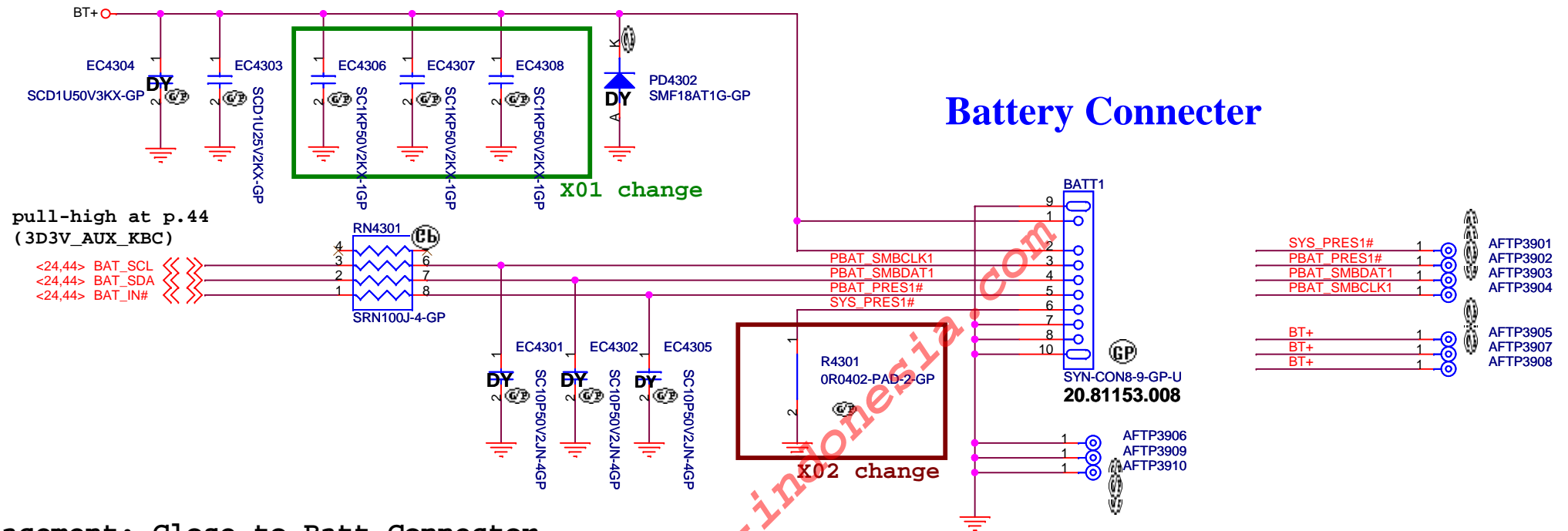


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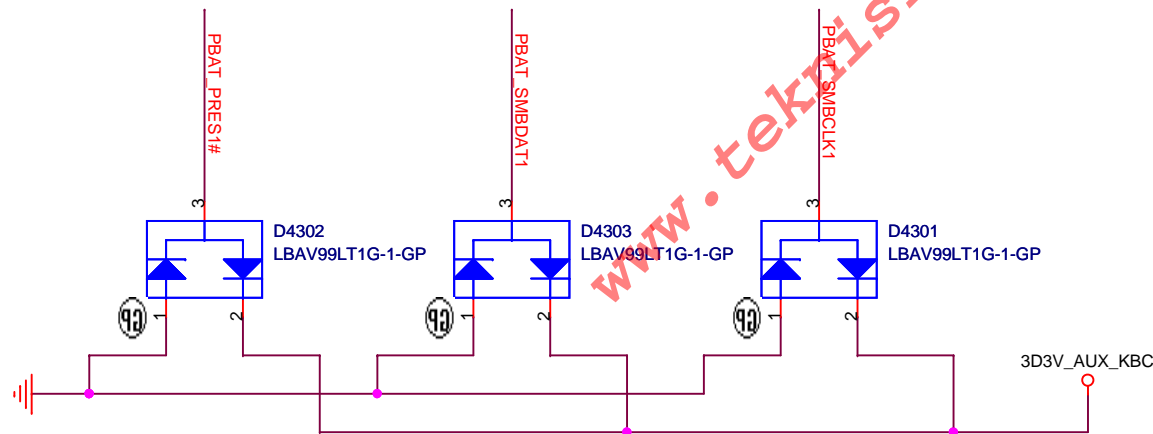


Title			
<b>DCIN JACK</b>			
Size A3	Document Number		Rev
	<b>Iris BTM</b>		<b>A00</b>
Date:	Monday, November 17, 2014	Sheet 42 of	102

# Main Func = M-BAT Input



Placement: Close to Batt Connector



75.00099.O7D  
2nd = 75.00099.K7D  
3rd = 75.00099.Q7D  
4th = 75.00099.D7D

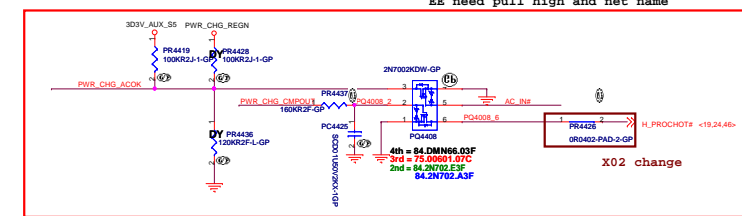
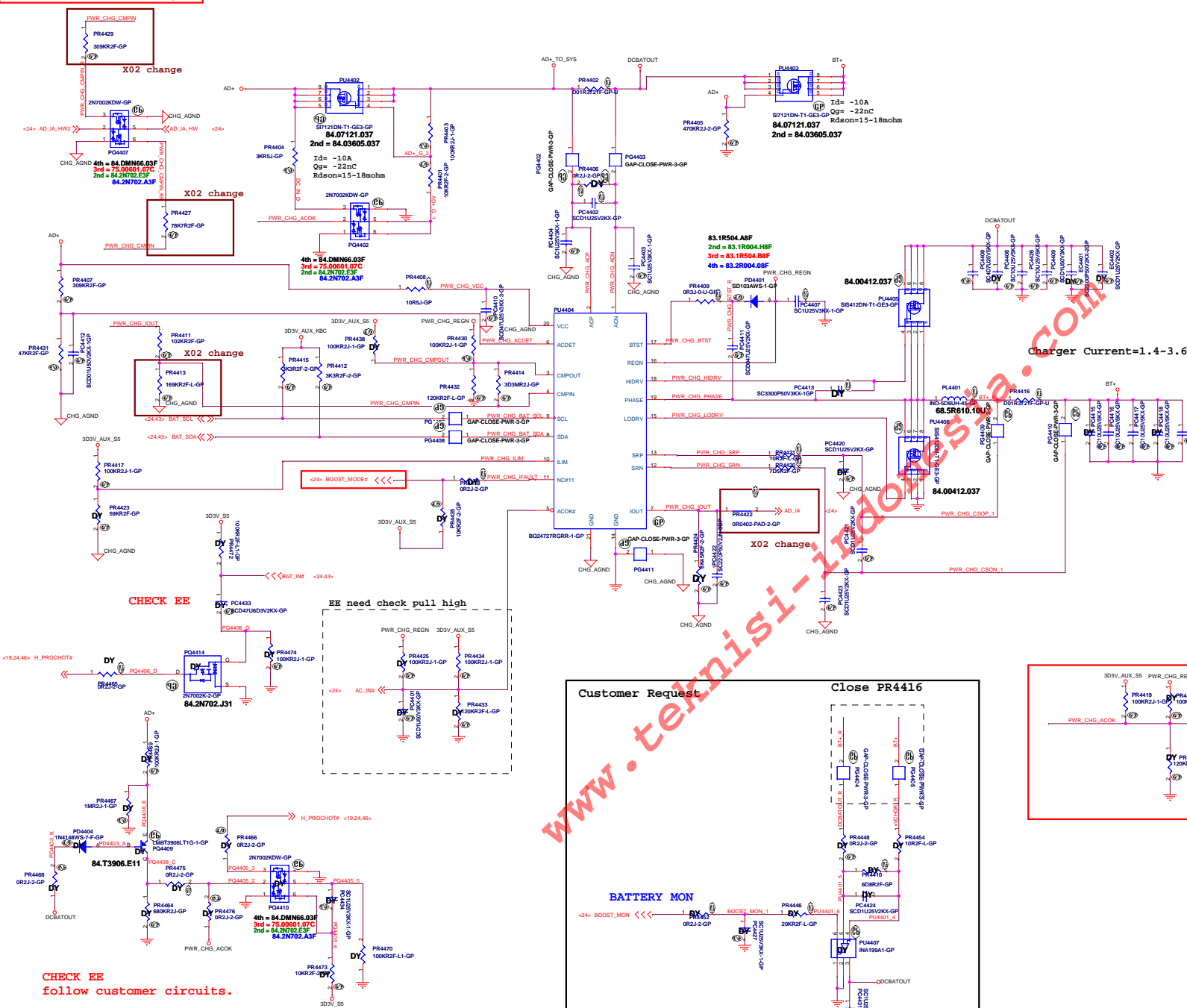
75.00099.O7D  
2nd = 75.00099.K7D  
3rd = 75.00099.Q7D  
4th = 75.00099.D7D

75.00099.O7D  
2nd = 75.00099.K7D  
3rd = 75.00099.Q7D  
4th = 75.00099.D7D

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Title <b>BATT CONN</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
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Main Func = Charger

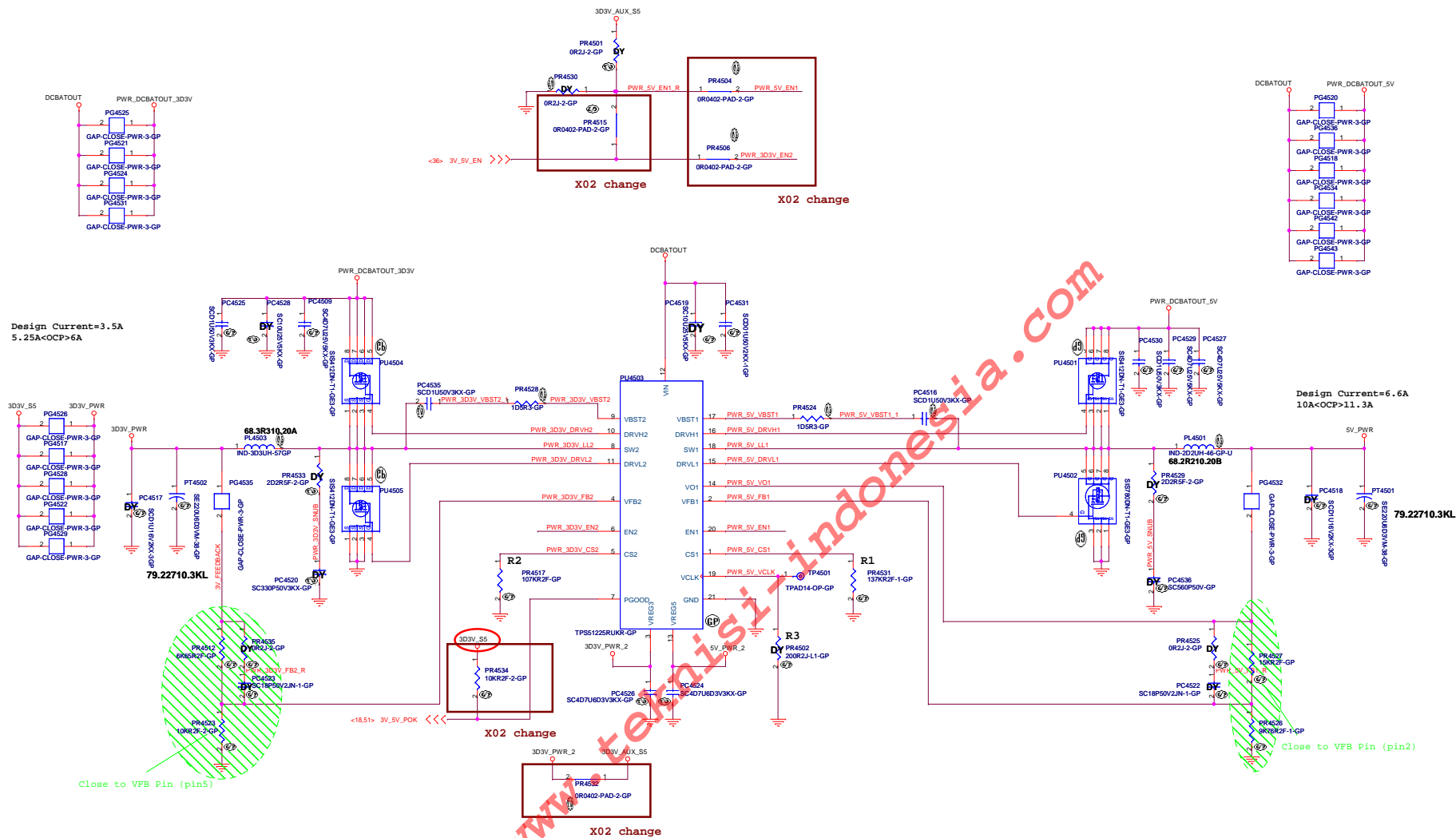


EC code only BQ24727

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
35W	0	0
45W	1	0
65W	0	1

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Main Func = 3D3V\_5V

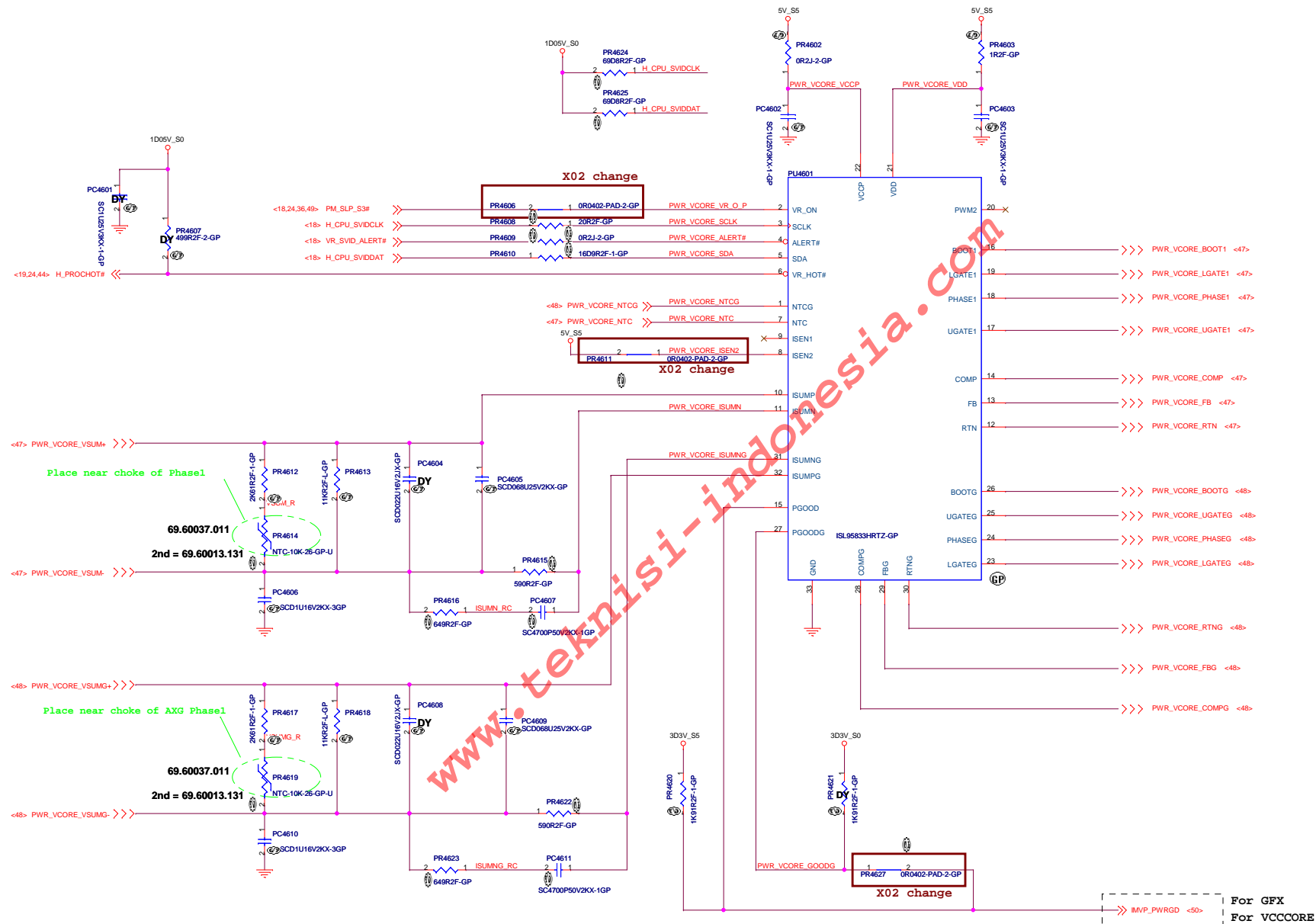


I/P cap: CHIP CAP C 10U 25V K0805 X5R / 78.10622.51L  
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap: CHIP CAP EL 220U 6.3V M6 3+4.4 / Chemi-con / 18mOhm / 79.22710.3KL  
H/S: SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S: SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R / 78.10622.51L  
Inductor: CHIP CHOK 2.2UH PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap: CHIP CAP EL 220U 6.3V M6 3+4.4 / Chemi-con / 18mOhm / 79.22710.3KL  
H/S: SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S: SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

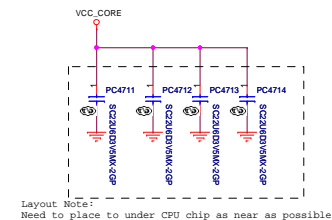
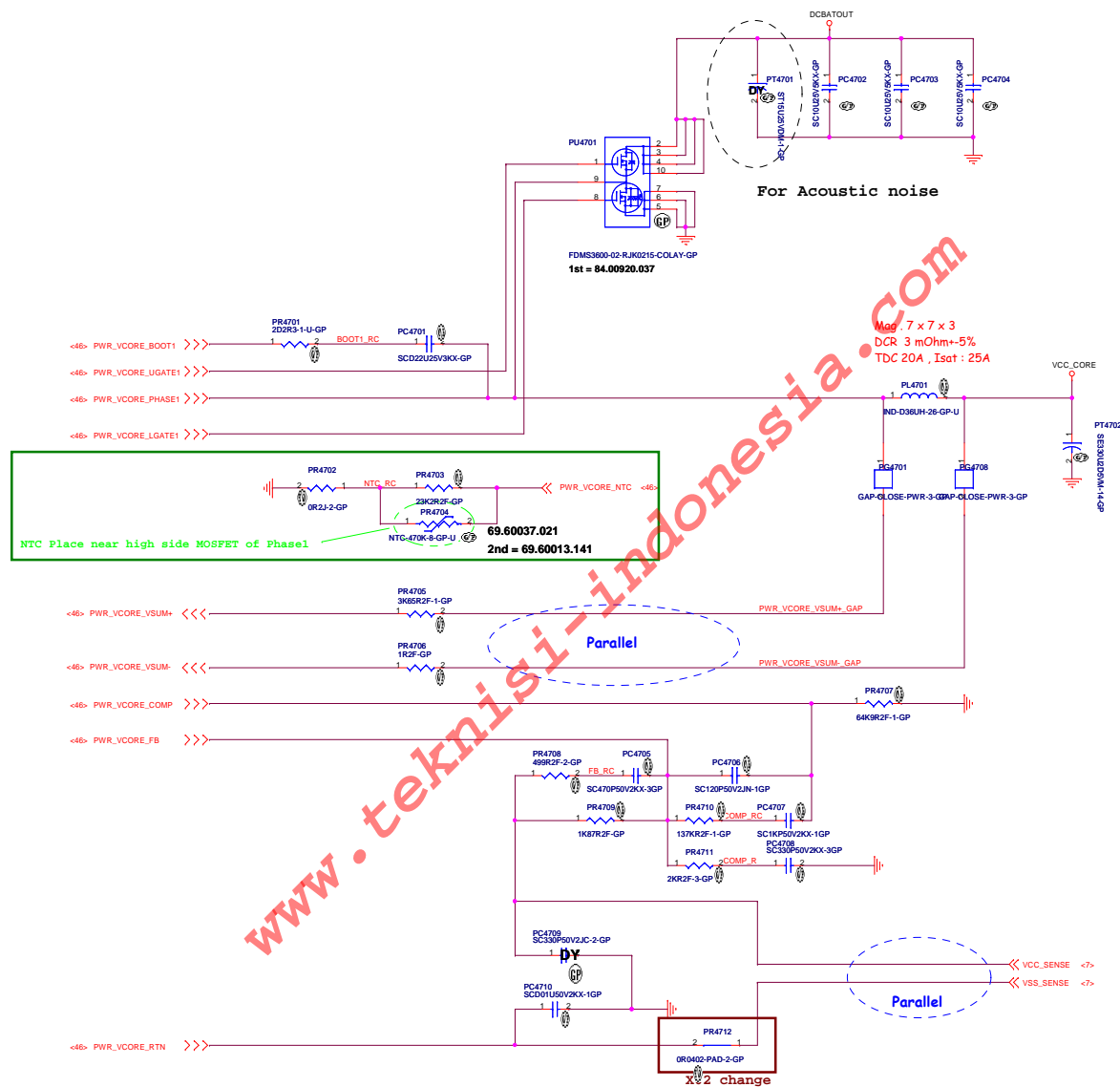
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**Main Func = CPU\_CORE**



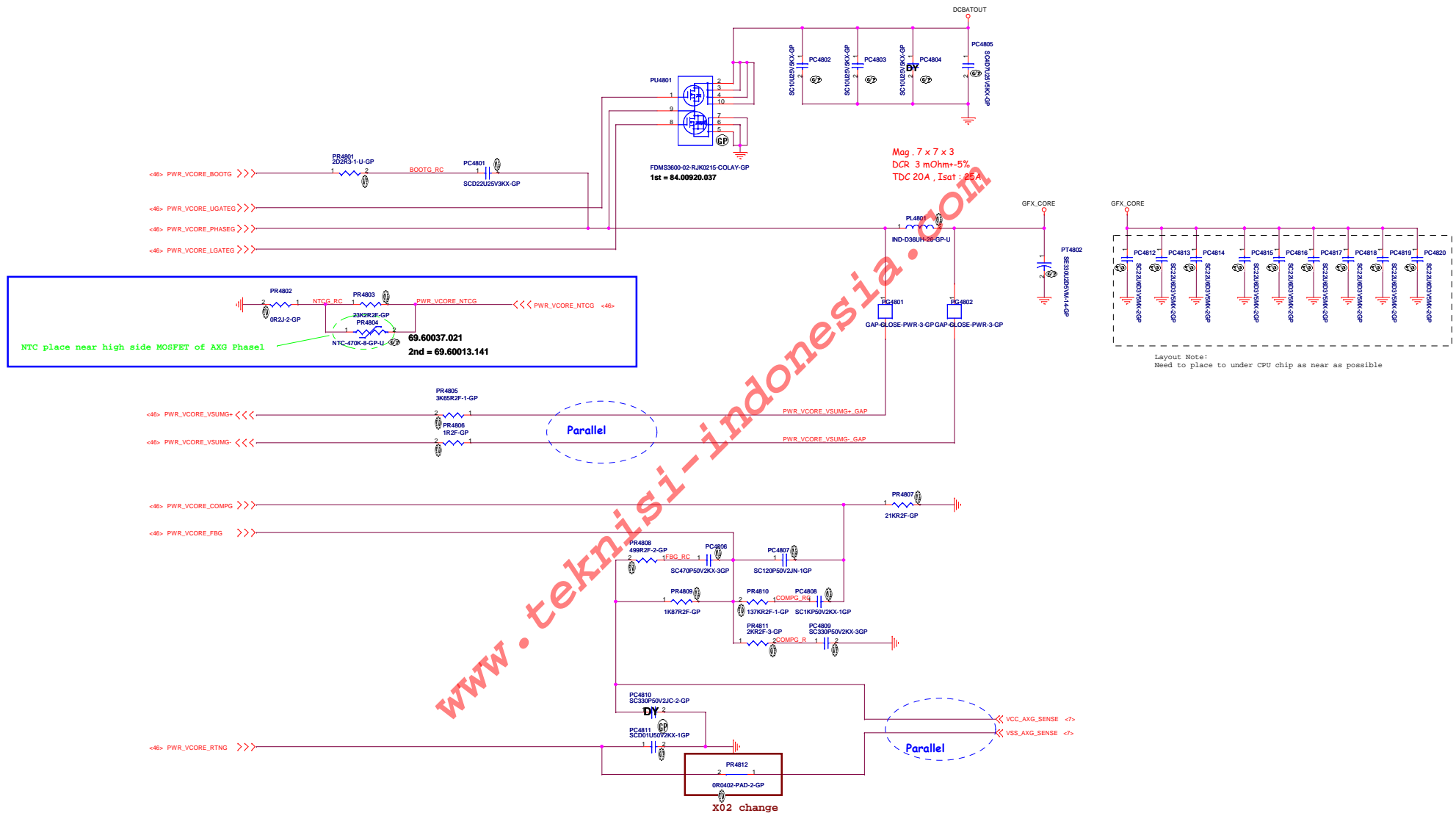
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Main Func = CPU\_CORE



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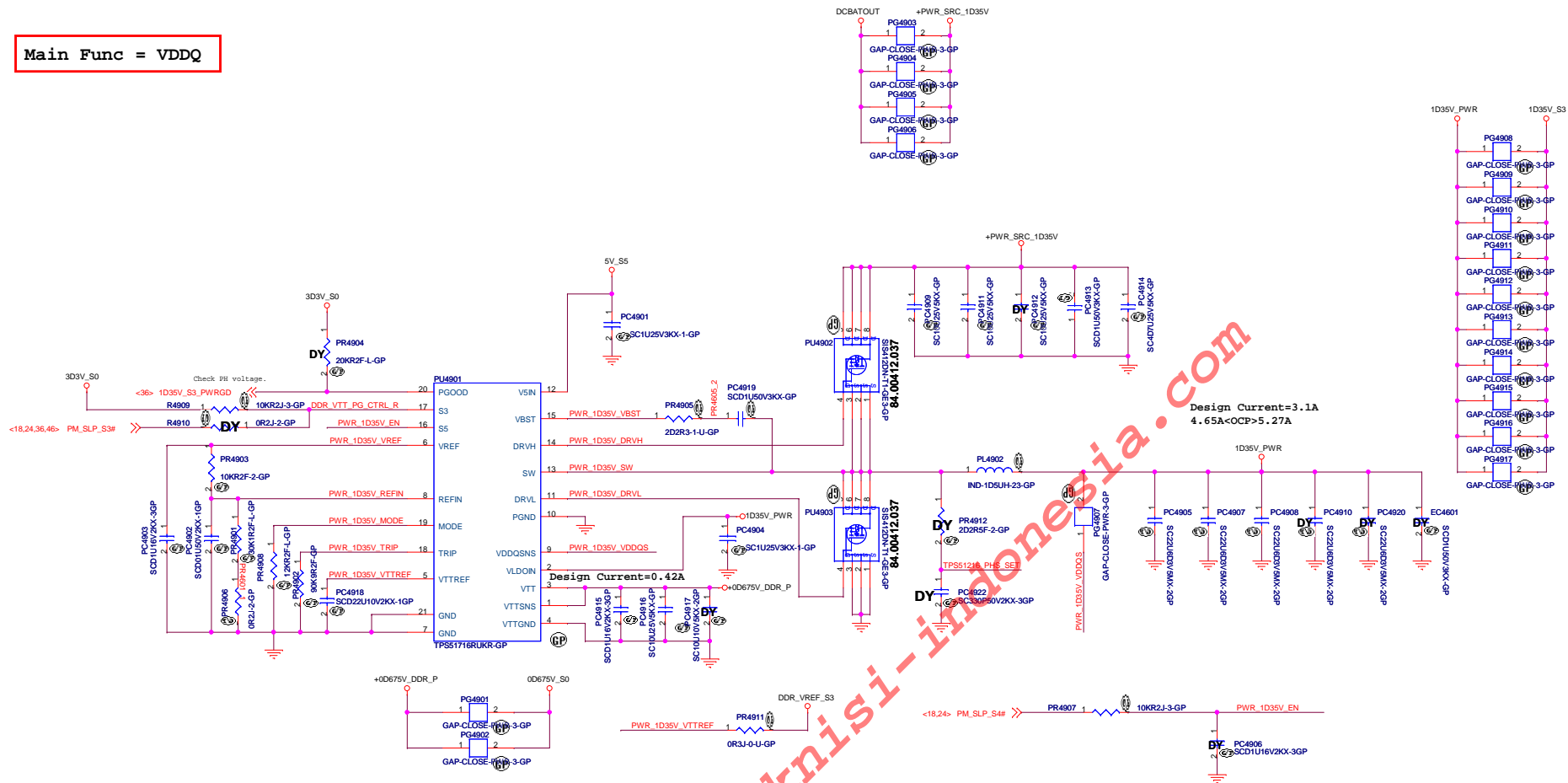
Main Func = CPU\_CORE



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Main Func = VDDQ



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

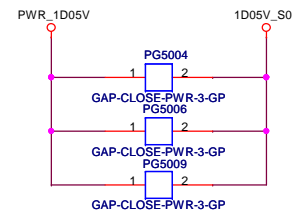
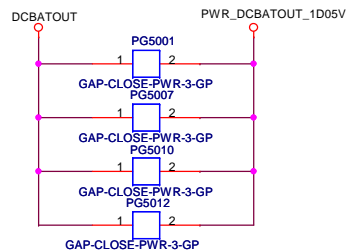
TP51716 MODE

PR4908	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

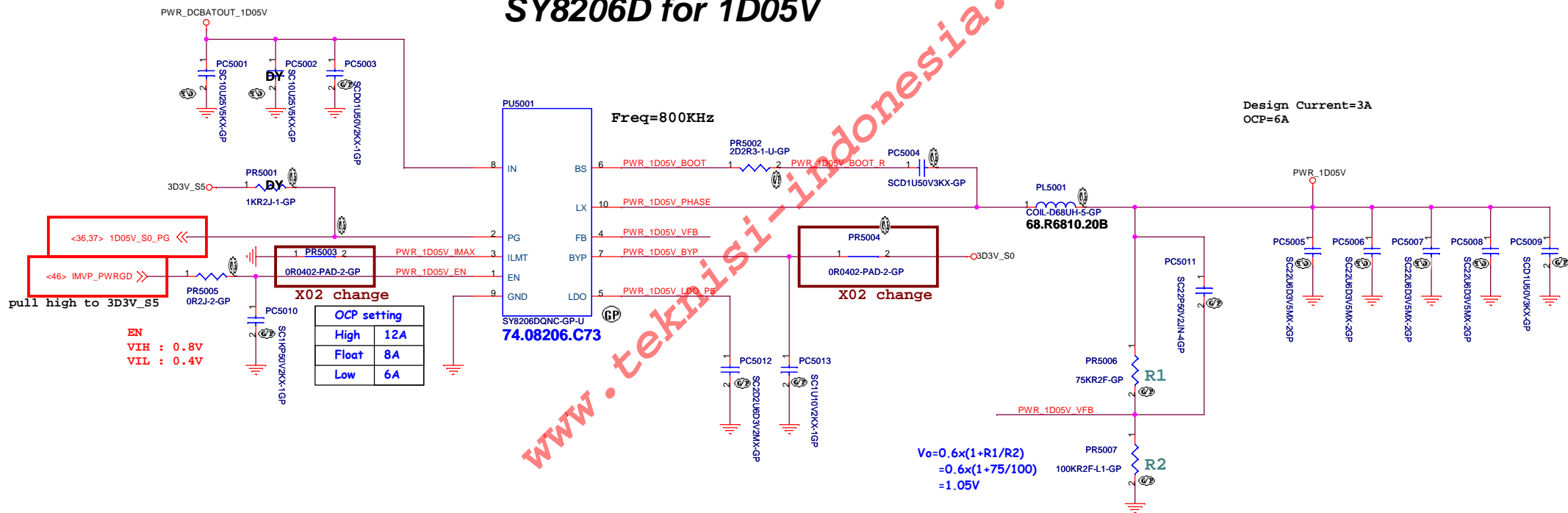
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
 Inductor: CHIP CHOKE 1.5U PCMC063T-1R5MN 14-15mohm Isat =18Arms 68.1R510.10K  
 B/S MOS: FET MOS SIS412DN-T1-GE3 NC 8P / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V  
 L/S MOS: FET MOS SIS412DN-T1-GE3 NC 8P / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V

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Main Func = 1D05V



## SY8206D for 1D05V

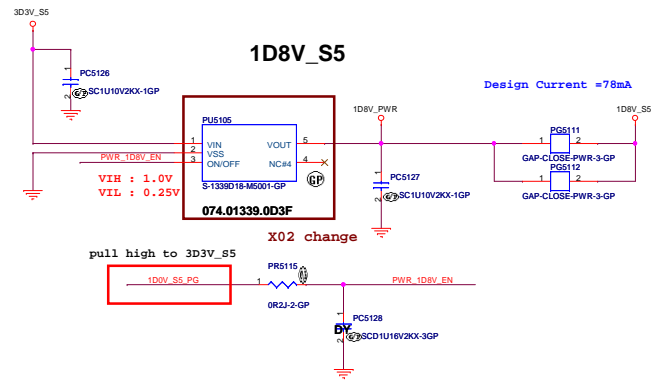


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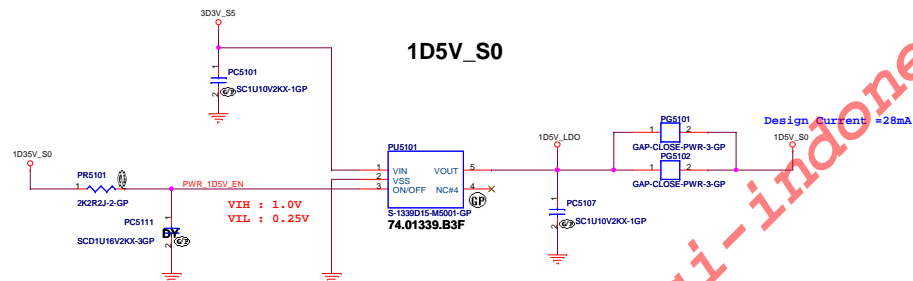
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Title  
**SY8206D DCDC 1D05V**  
Size A3 Document Number  
**Iris BTM** Rev  
**A00**  
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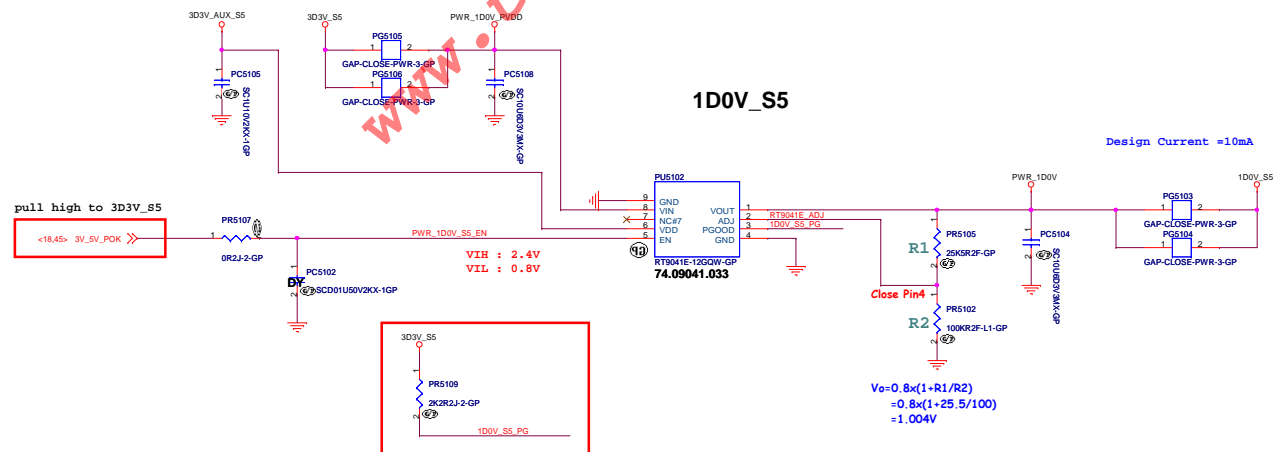
Main Func = 1D8V



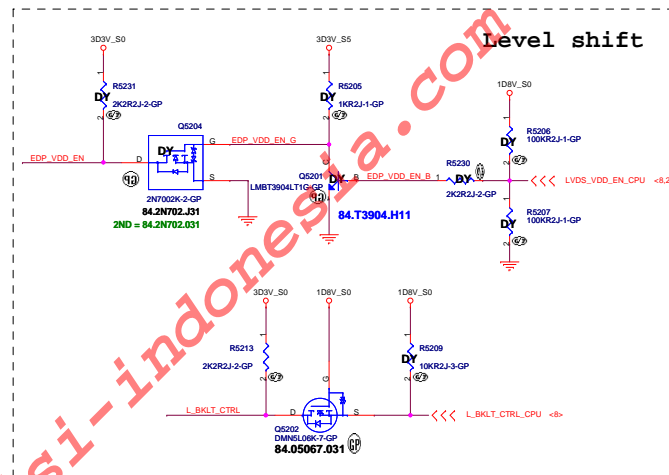
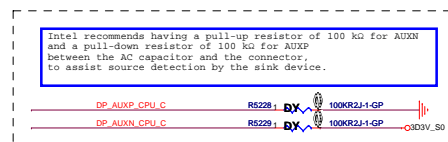
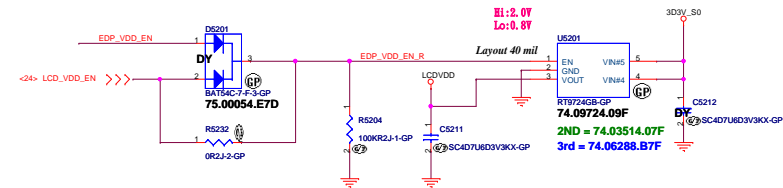
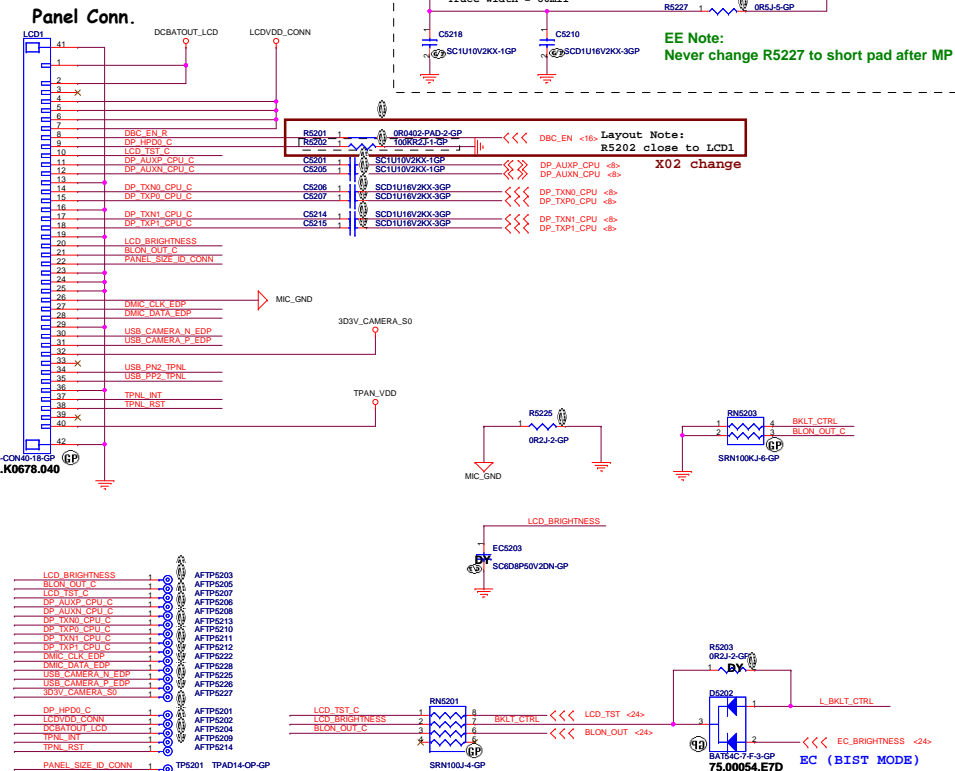
Main Func = 1D5V



Main Func = 1D0V

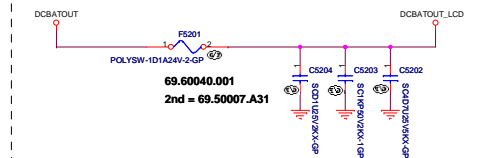


**Main Func = LCD**



### INVERTER POWER

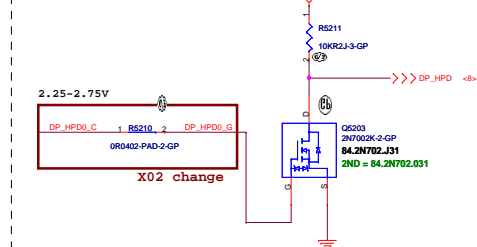
**EE Note:**  
**Never change R5208 to short pad after MP**



```

| EE Note:
| Need to check LCD Panel spec for
| HPD voltage level.
|
| Layout Note:
| Place PL resistor of DP_HPD0_C close to LCD1.

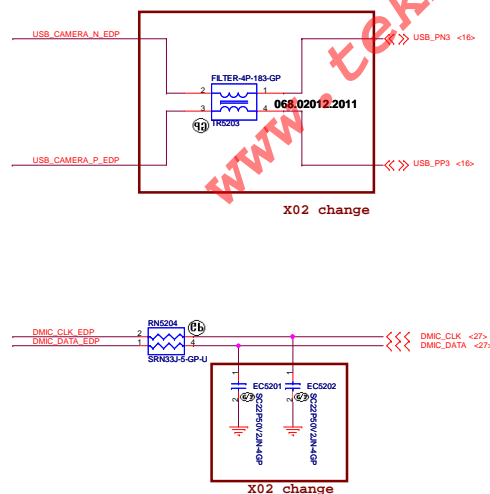
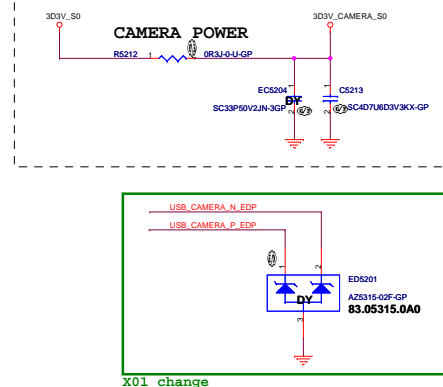
```



**Main Func = Camera + DMIC**

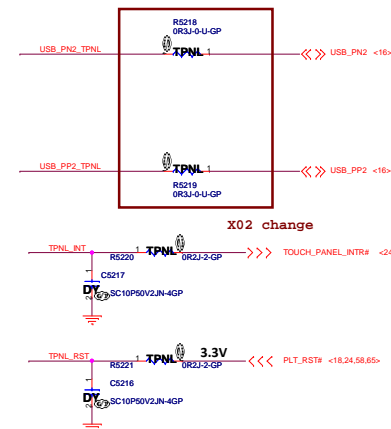
## Camera + Microphone

**EE Note:**  
**Never change R5212 to short pad after MP**

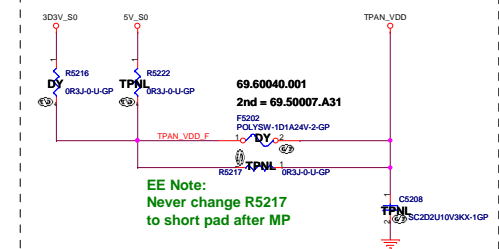


**Main Func = TS**

## Touch Screen



## TOUCH PANEL POWER



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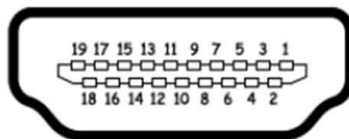
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Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
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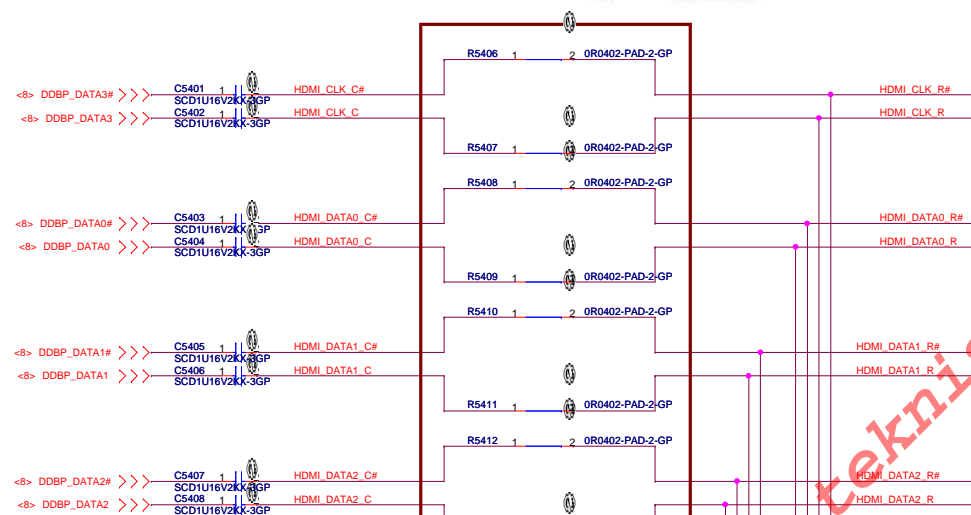
Main Func = HDMI

# HDMI Level Shifter & Connector

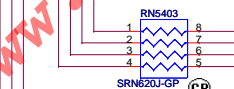


Reserve 150 ohm bridge resistance on the HDMI trace as circle for EMI.

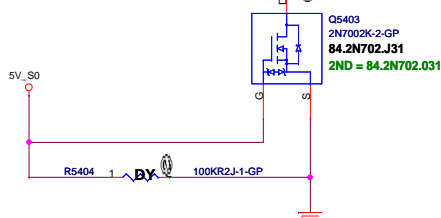
Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		



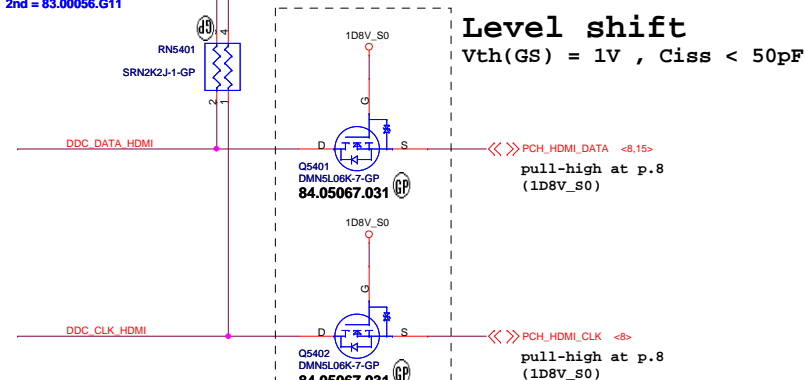
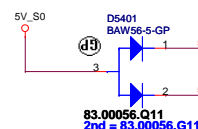
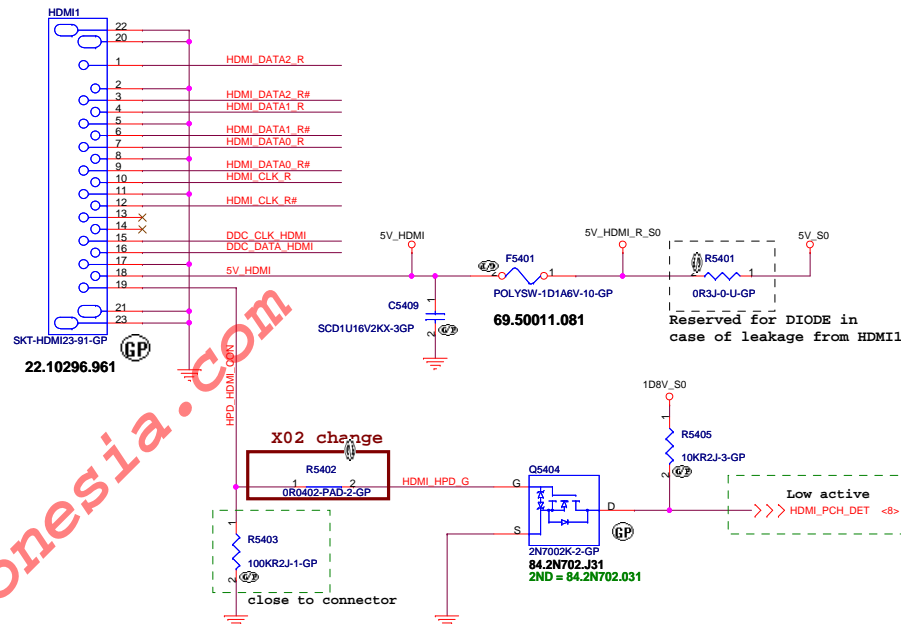
X02 change



PDG(#512238): 620  $\Omega$   $\pm$ 5%



## HDMI Connector




Level shift  
 $V_{th}(GS) = 1V$ ,  $C_{iss} < 50pF$

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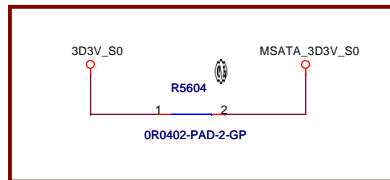
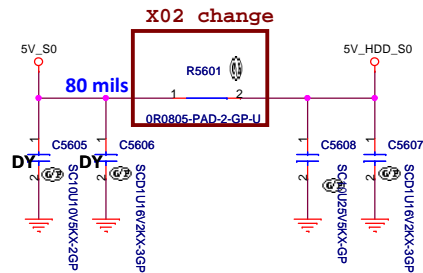
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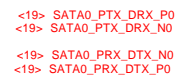
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number		Rev <b>A00</b>
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**Main Func = HDD**

## SATA HDD Connector

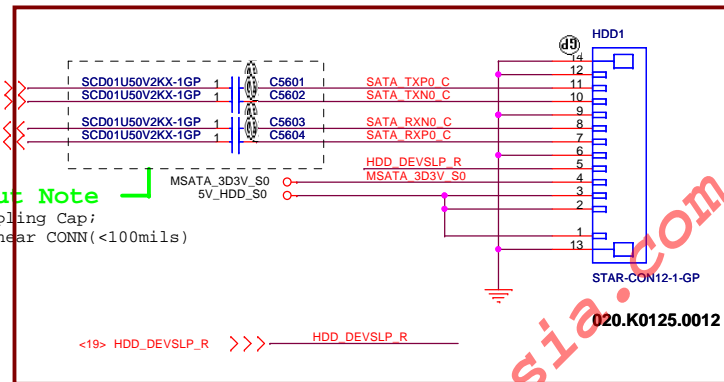


x02 change



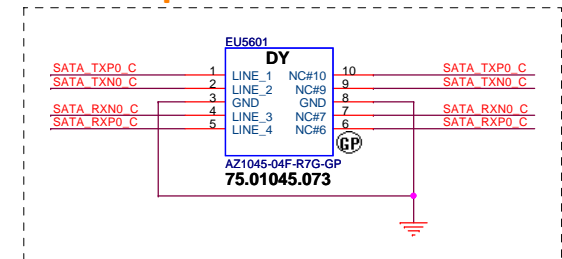
**Layout Note** —

AC coupling Cap;  
place near CONN(<100mils)



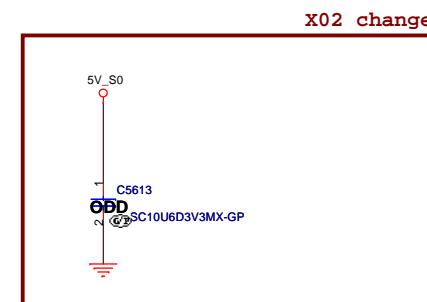
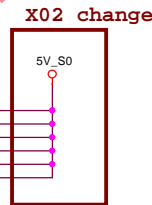
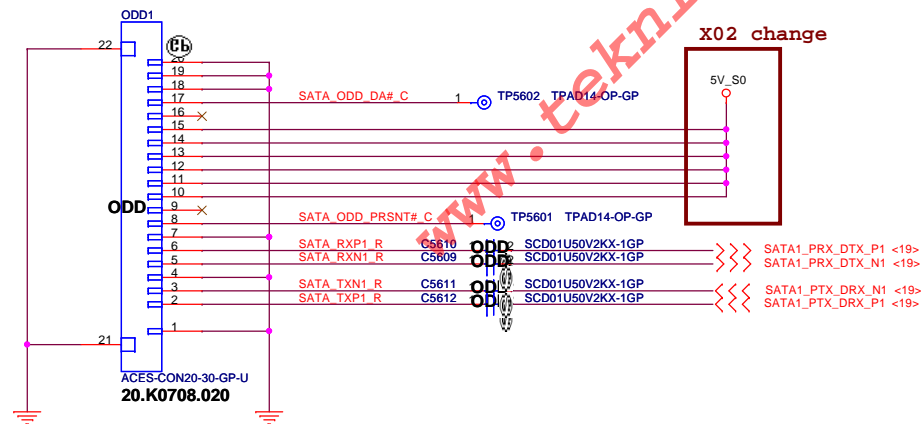
x02 change

## EMI Request



**Main Func = ODD**

## ODD Connector




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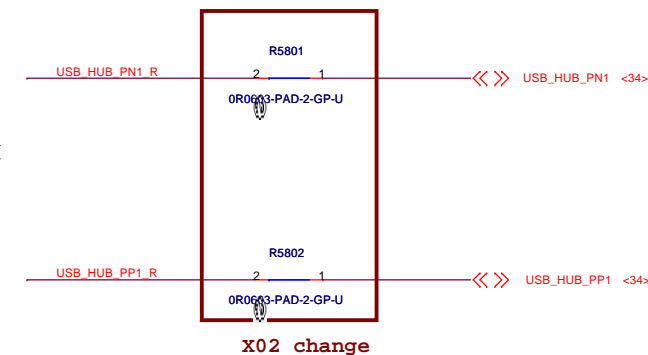
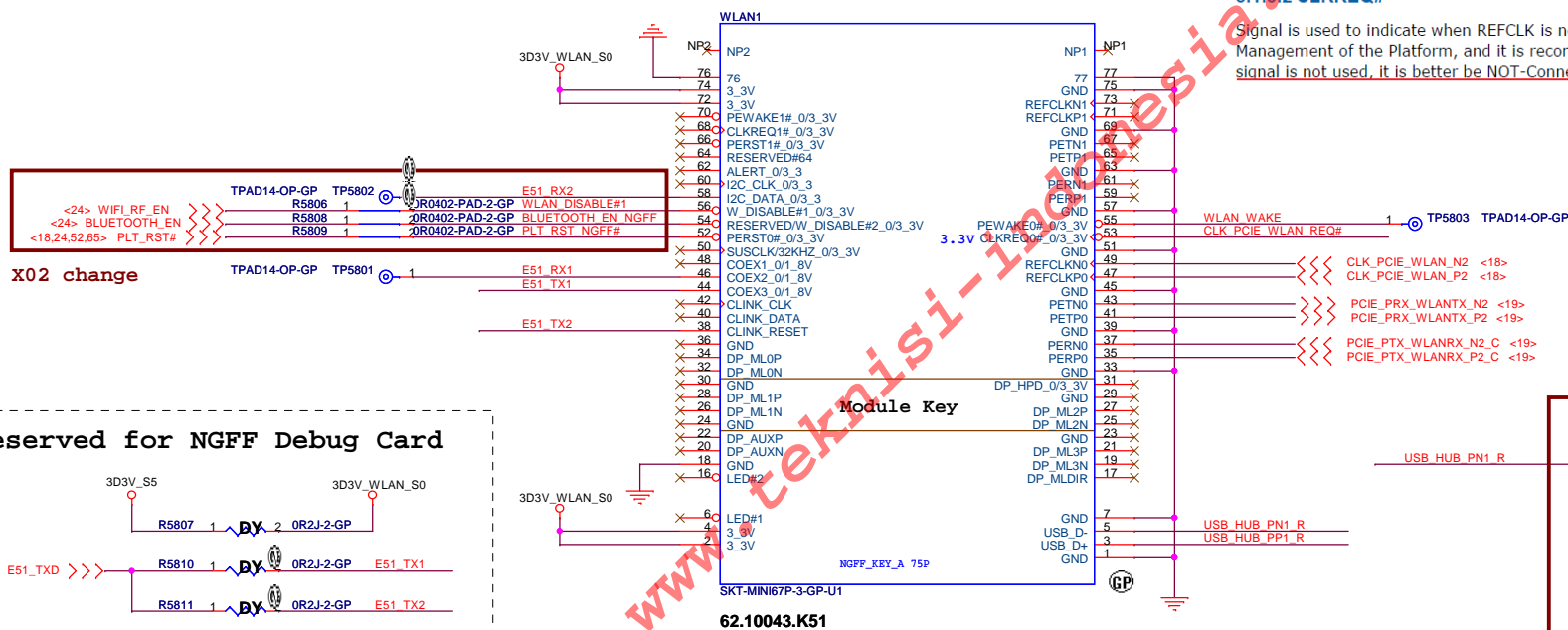
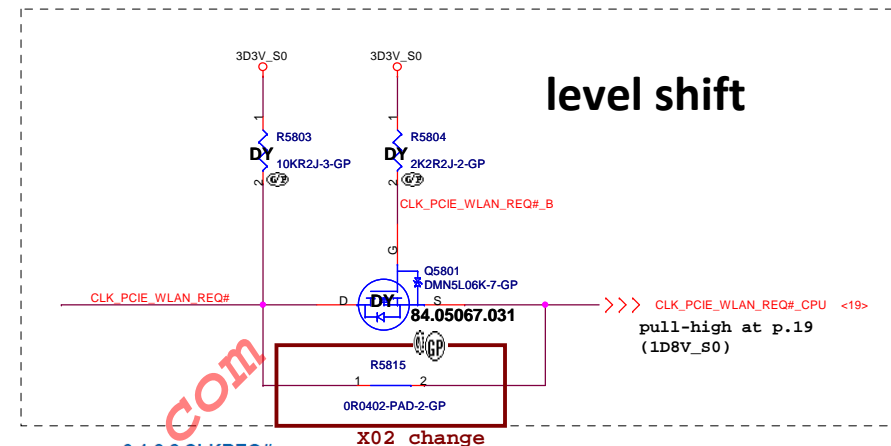
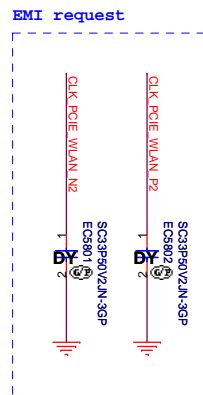
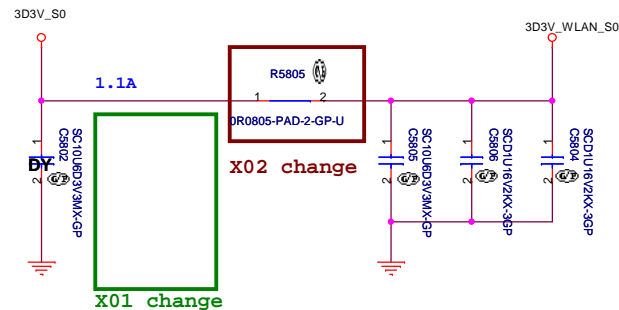
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**Main Func = WLAN**



Reserved for NGFF Debug Card

EE Note:  
For NFGG Debug Card:  
Stuff R5807,R5810,R5811(optional).  
DY R5805.

AFTP5801	1	3D3V WLAN S0
AFTP5802	1	CLK PCIE WLAN REQ#
AFTP5803	1	WLAN DISABLE#1
AFTP5804	1	BLUETOOTH EN NGFF
AFTP5805	1	PLT RST NGFF#
AFTP5806	1	USB HUB PN1 R
AFTP5807	1	USB HUB PP1 R

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**WLAN CONN**

Size

Document Number
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Date

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Date \_\_\_\_\_

Main Func = WWAN/mSATA

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Main Func = mSATA

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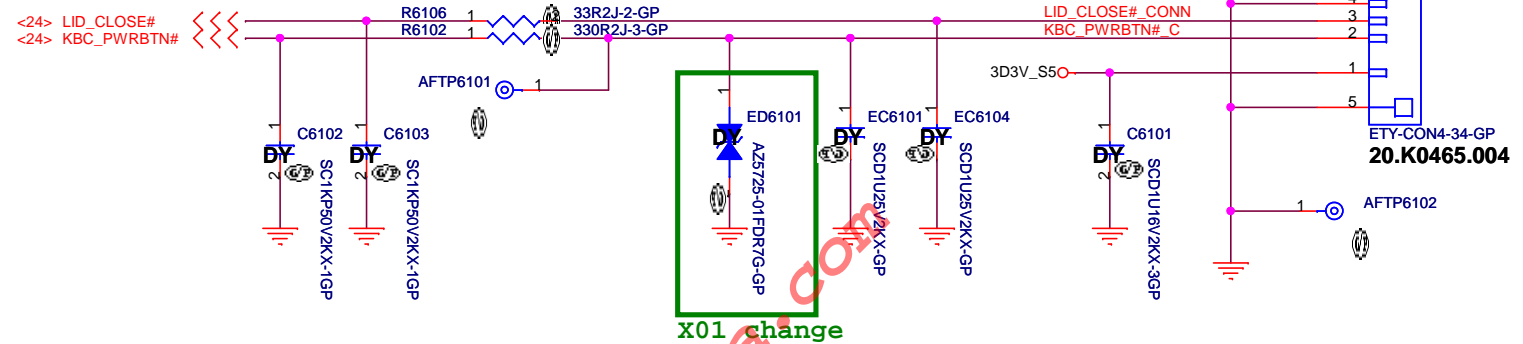
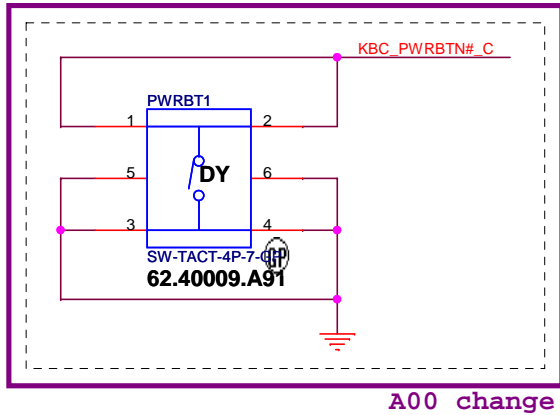
# Blanking

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## Main Func = Power BTN

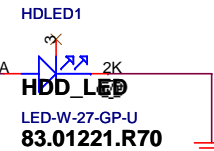
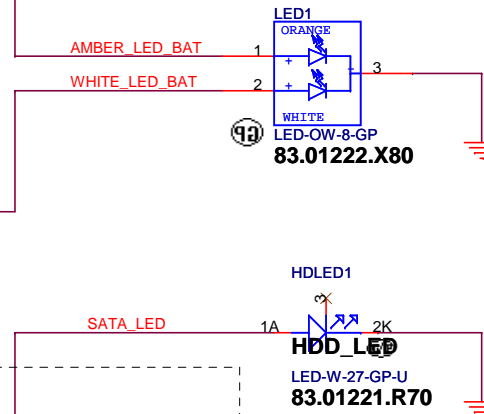
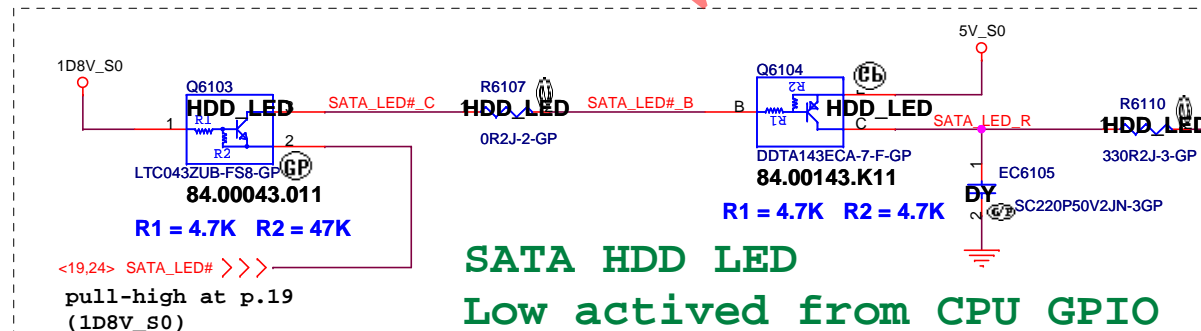
## Power Button & Hall Sensor



## Main Func = LED

Battery LED1  
Low activated from KBC GPIO

Battery LED2  
Low activated from KBC GPIO



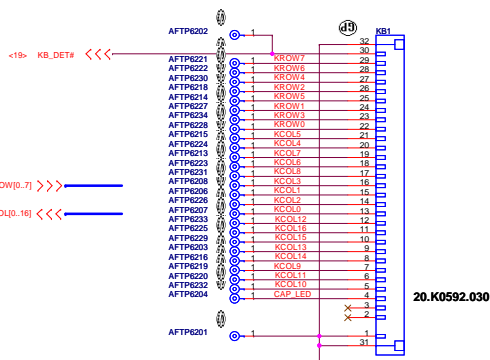
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LEDBard/PowerButton			
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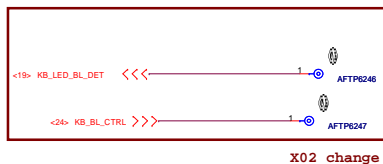
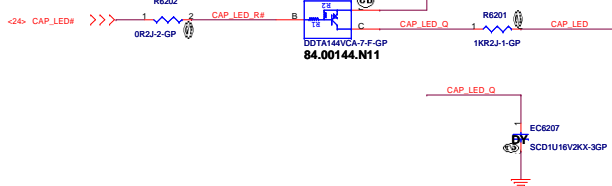
Main Func = KB

## Keyboard

### Internal Keyboard Connector (14")

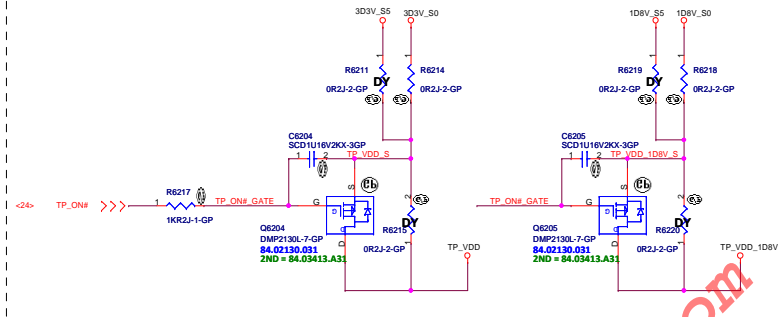


### CAP LED Control LOW active from KBC GPIO

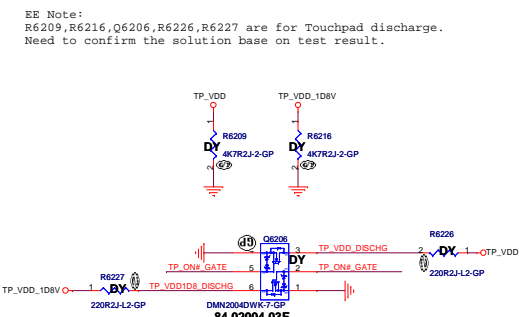


Main Func = TPAD

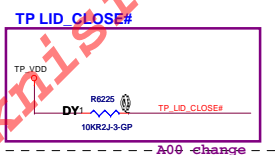
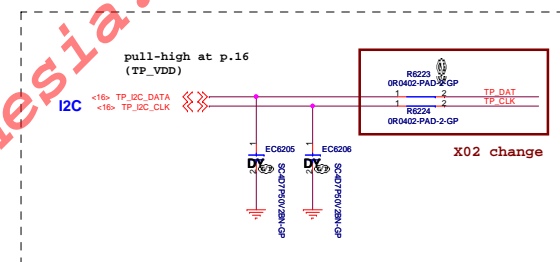
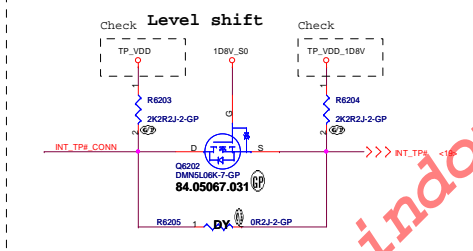
### Touchpad Power



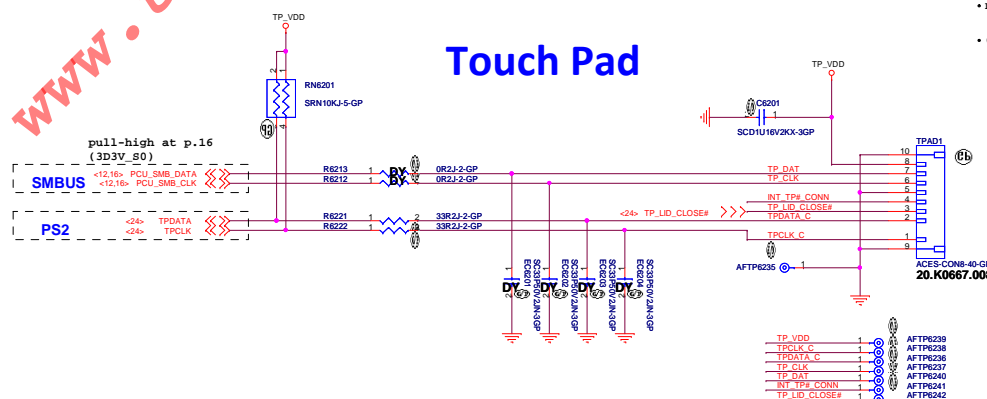
### Touchpad Power Discharge



### INT#



## Touch Pad

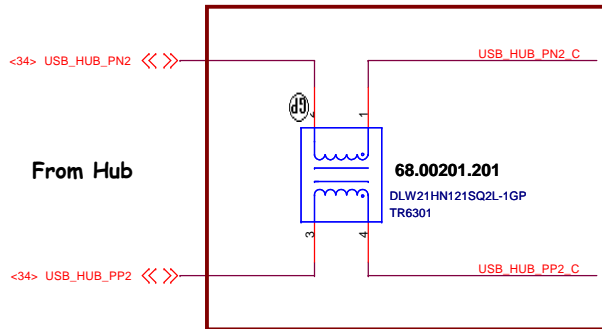


- (#514849) I2C PTP Pins
- Standard I2C pins for interrupt driven I2C device:
- +3.3V VDD
  - GND
  - SCL (clock)
  - SDA (data)
  - INT# (or INTR#, interrupt), also known as ATTN# (attention)
- Other pins needed on I2C PTP:
- wake# - level trigger signal from PTP to Host
  - Overload the INTR#/ATTN# line (on the same pin)
  - Only used during S3
  - Active low
  - Connect to either wake capable mechanism on chipset
  - GPIO pin (suspend Well powered) for S3 platform
  - GPIO on EC (and route to GPIO27 or PWRBTN# on chipset)
  - DSW (interrupt disable)
  - level trigger signal from sensor (slate mode decider) to PTP
  - Active low (active = disable any interrupt, including wake)
  - (Optional) +1.8V VDD

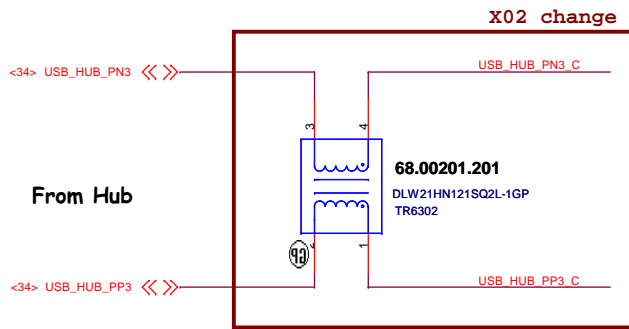
Pin No.	Pin name
1	VDD (3.3V)
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	INT#
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

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Main Func = IO Connector



USB2 (USB2.0) CMC



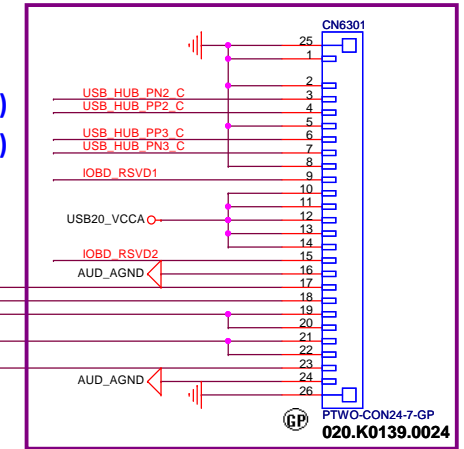
USB3 (USB2.0) CMC

X02 change

## I/O Board Connector

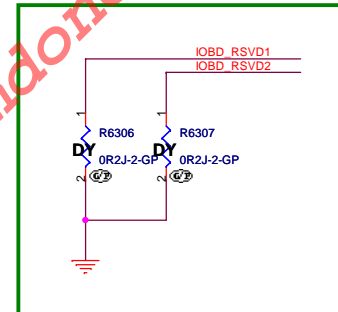
USB2 (USB2.0)  
USB3 (USB2.0)

<29> AUD\_PORTA\_L\_R\_B  
<29> AUD\_PORTA\_R\_R\_B  
<29> SLEEVE\_R  
<29> RING2\_R  
<29> JACK\_PLUG

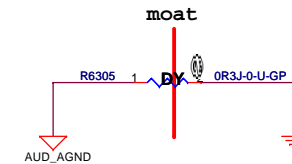


A00 change

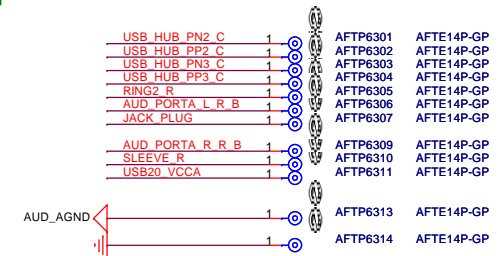
Universal Jack



X01 change



Pitch: 1mm  
Power: 5 pins  
GND: 4 pins  
AGND: 2 Pins



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IO Board Connector		
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Main Func = Hall Sensor

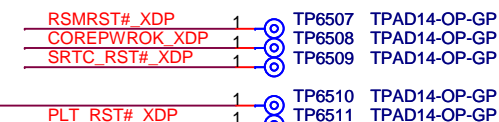
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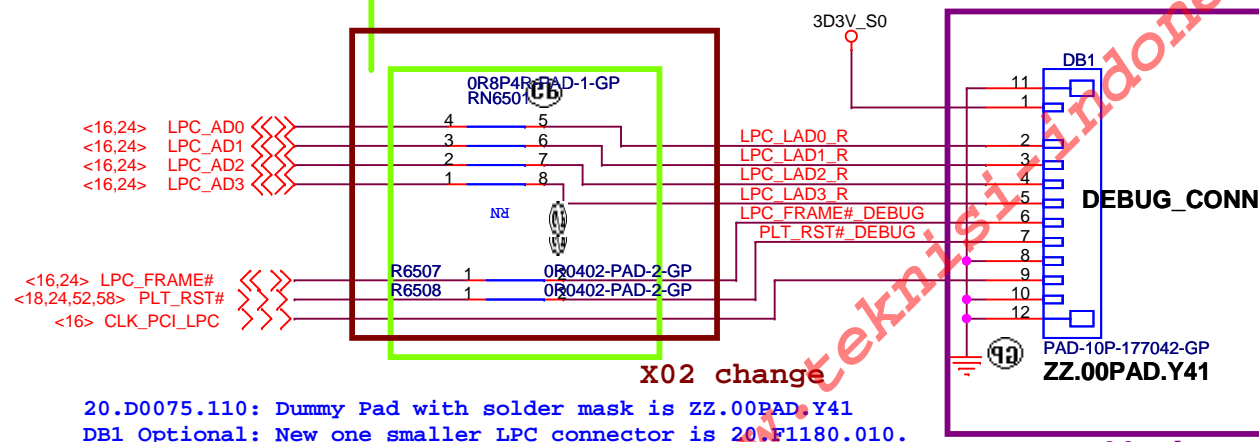
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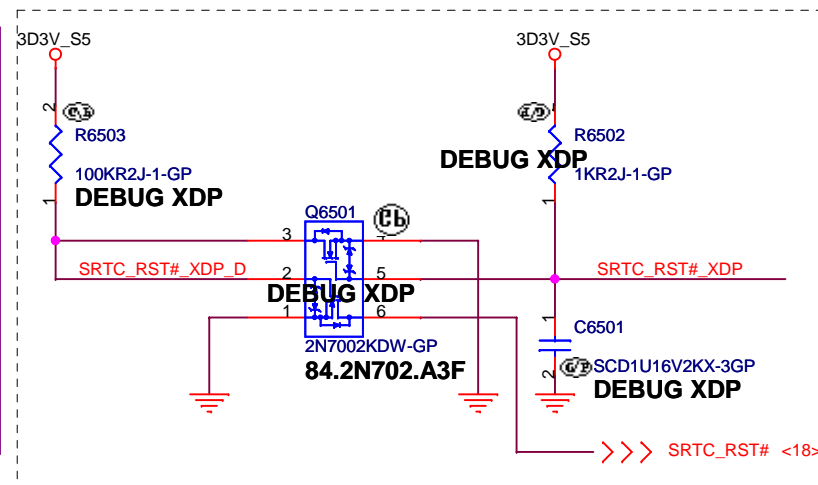


Place near trace separated point



X02 change

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41  
DB1 Optional: New one smaller LPC connector is 20.F1180.010.



Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title

## Debug connector

Size  
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Main Func = Sensor Hub+Accelerometer (G-Sensor)+Gyro+Proximity SAR+ALS

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Main Func = G-Sensor

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Main Func = Thunderbolt

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Main Func = dGPU

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Main Func = dGFX\_CORE

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Main Func = GFXLCD

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Main Func = GFXCRT

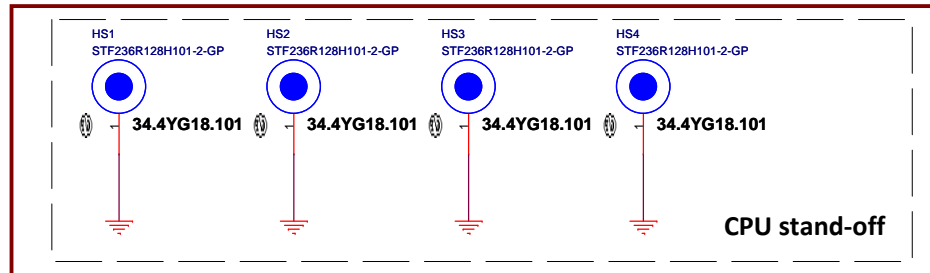
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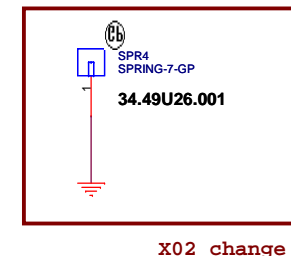
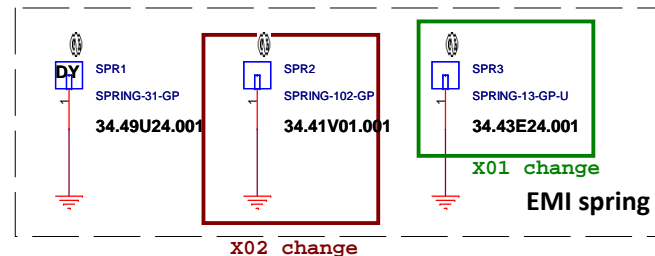
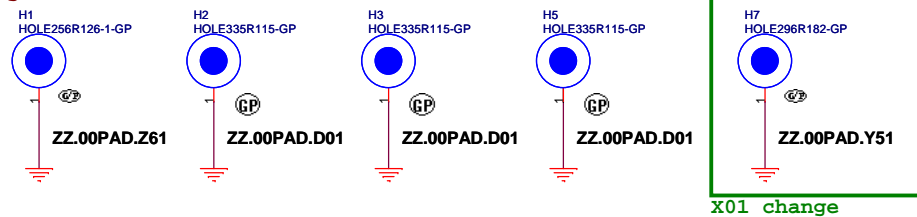
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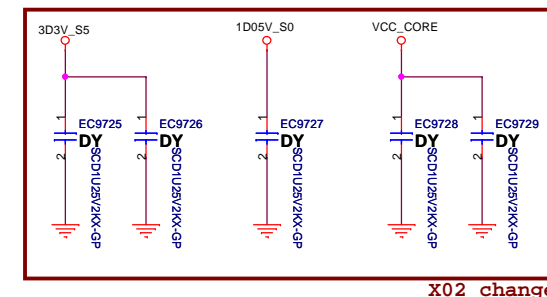
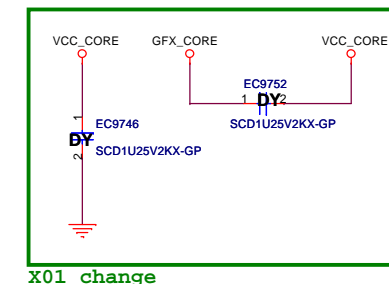
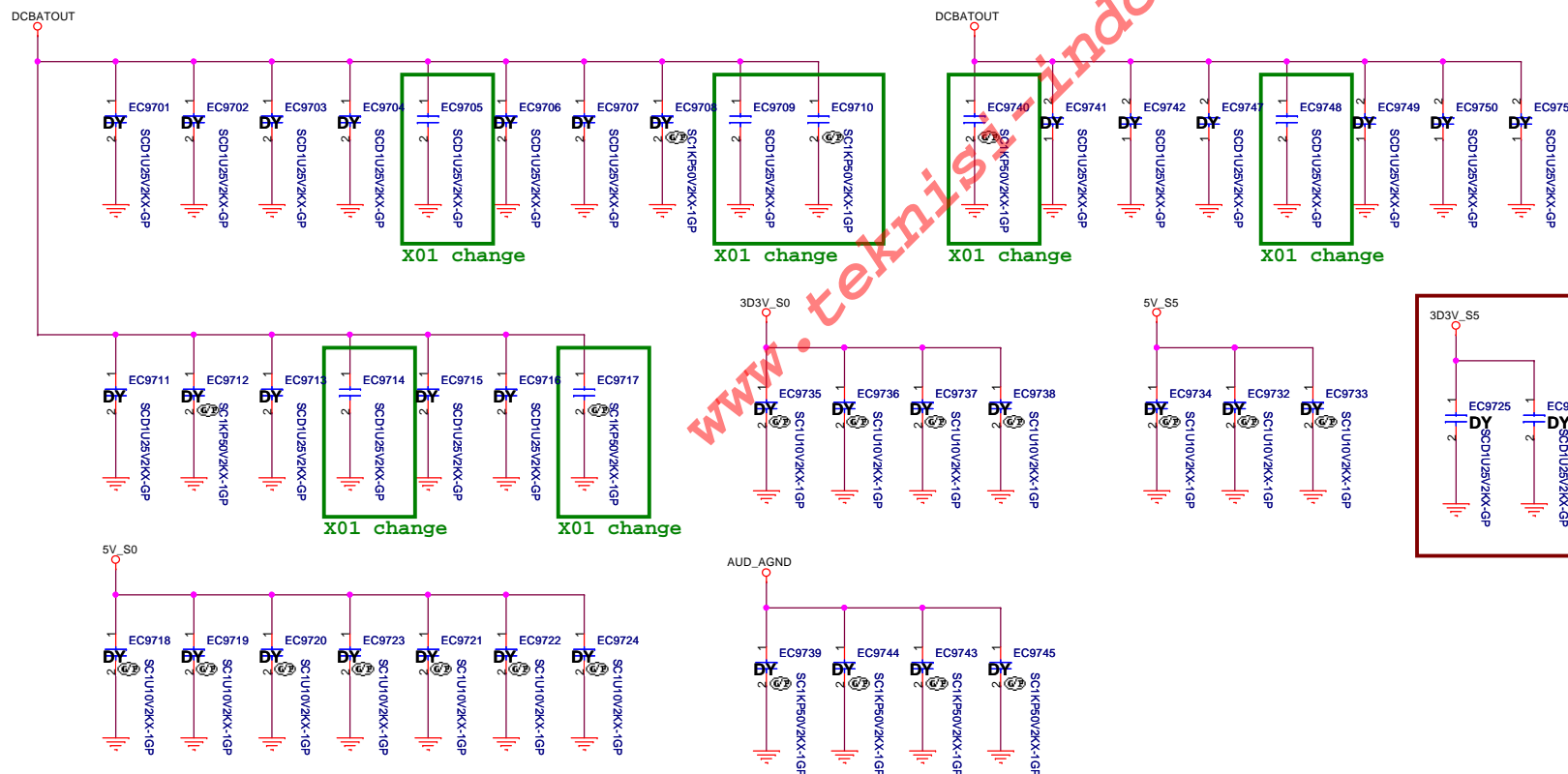
## Main Func = Unused Parts



X02 change



## Main Func = EMI Capacitors




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Main Func = NFC

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Main Func = TPM

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Main Func = FPR

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Main Func = SmartCard

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Main Func = SmartCard

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Main Func = Switchable

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Main Func = Dock

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## Change History

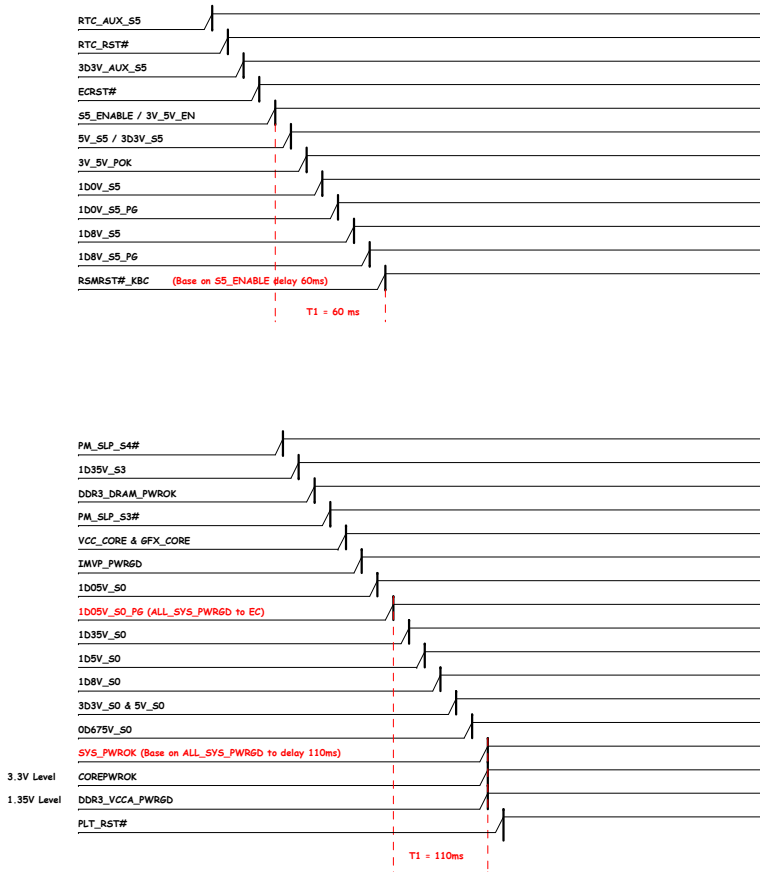
Ver.	Date	Page	Change Description	Reasons
X00	06/18	18	Change C1806, C1807 to 7pF	CPU 32K Xtal fix. (X1802)
X00	06/18	34	Change C3415, C3416 to 22pF, add R3426.	USB hub 12M Xtal fix. (X3401)
X01	08/12	86	Add H7.	Dell ME and UI request.
X00	06/18	35	Mount R3502, R3505, dummy U3505, C3518.	No layout space for adding H7.
X00	06/18	51	Change PU5102.6 to 3D3V_AUX_S5.	Fix power down sequence. (1D0V_S5_PG)
X00	07/01	24,62	Mount R2408 and R6225.	Touchpad lid close function.
X00	07/01	24,26	Mount R2468 and R2603, dummy R2601.	Use KBC T8.
X01	07/31	24	Add R2438.	SATA LED indicate.
X01	07/31	37	Reserve R3704, R3705.	Reserve 1.5V bypass to 1.8V.
X01	07/31	52	Reserve ED5201.	ESD protection for MP.
X01	07/31	56	Add R5604.	mSATA power.
X01	07/31	63	Reserve R6306, R6307.	ESD protection for CM mode.
X01	08/04	54	Reserve TR5401~TR5404.	EMI for CM mode.
X01	08/11	58	Delete C5801, C5803.	No layout space for adding H7.
X01	08/11	61	Reserve ED6101.	EMI for power BTN.
X01	08/11	86	Reserve EC9746, EC9752.	EMI for CM mode.
X01	08/12	29	Mount EC2901~EC2904	EMI request for speaker noise.
X01	08/12	43	Add EC4306~EC4308.	EMI request for BT+ power noise.
X01	08/12	86	Mount EC9705, EC9709, EC710, EC9714, EC9717, EC9740, EC9748 and SPR3.	EMI request for DCBATOUT power noise.
X01	08/14	24	Reserve Q2405, R2470.	SATA/WHITE LED switch.
X01	08/27	34, 52, 63	Change TR3401, TR5203, TR6301, TR6302 to 068.02012.2011.	EMI request for USB noise.
X02	09/22	44	1. Change PR4413 to 169kohm. 2. Change PR4429 to 309kohm. 3. Change PR4427 to 78.7kohm.	Power team request for 35W power companion.
X02	09/26	24	change R2424 from 64.33025.6DL (33k) to 64.47025.6DL (47k)	PCB Version
X02	09/26	45	change PR4534 from 63.10434.1DL (100k) to 64.10025.6DL (10k)	Correct 3V_5V_POK 2.7V to 3.3V
X02	09/26	24	dummy R2438 ; stuff R2471,Q2405	For ROSA HDD LED Function
X02	09/26	86	HS1~HS4 change from 34.4Z003.201 to 34.4YG18.101	Use stand off without mylar
X02	09/26	19,56	add R1915, R1908, Q1901, CPU1.BA24 (SATA_DEVSPLP_0) add HDD1.5(HDD_DEVSPLP_R)	DEVSPLP Function
X02	09/29	51	PU5105 change from 74.01339.D3F to 074.01339.0D3F	tape direction (power IC)
X02	09/29	56	HDD connettor change from 020.K0016.0012 to 020.K0125.0012	change PTH type
X02	09/29	34,52, 63	TR3401 ( 068.02012.2011 ) :SWAP TR5203 ( 068.02012.2011 ) :SWAP TR6301 ( 068.02012.2011 ) :SWAP TR6302 ( 068.02012.2011 ) :SWAP	CMC change from 68.00201.201 to 068.02012.2011
X02	10/01	19	del RN1903, CPU1.BB5 ; CPU1.BB7 change to connect GND	Layout space
X02	10/01	25	del SKT25	delete co-layer
X02	10/01	32	del TR3201	delete co-layer
X02	10/01	34	del R3401 R3402 ; TR3402, TR3403, TR3405	delete co-layer
X02	10/01	52	del R5223 R5224 ; TR5202	delete co-layer

Ver.	Date	Page	Change Description	Reasons
X02	10/01		RN2701 RN802 change from 66.R0036.04L to ZZ.0R04P.ZZZ	change to short pad
X02	10/01		R5601 R5805 change from 63.R0031.16L to ZZ.00PAD.M31	change to short pad
X02	10/01		RN6501 change from 66.R0036.A8L to ZZ.0R08P.ZHH	change to short pad
X02	10/01		R2706 R2906 R2907 R2909 R2911 R2405 R2703 R2704 R2711 R2901 R2902 R2903 R2904 R3201 R3202 R3414 R3415 R5801 R5802 change from 63.00000.00L to ZZ.00PAD.M21	change to short pad
X02	10/01		PR4422 PR4426 PR4504 PR4506 PR4515 PR4532 PR4627 R1203 R1207 R1210 R1211 R1827 R1832 R1836 R1924 R1925 R1928 R1929 R2102 R2104 R2408 R2410 R2414 R2416 R2427 R2429 R2430 R2434 R2453 R2460 R2461 R2507 R2509 R2510 R2511 R3102 R3303 R3304 R3305 R3306 R3619 R4301 R5201 R5210 R5402 R5806 R5808 R5809 R6223 R6224 R6507 R6508 R701 PR4606 PR4611 PR4712 PR4812 PR5003 PR5004 R1608 R1611R1614 R1615 R1616 R1818 R2415 R2419 R2422 R2441 R2449 R2465 R2467 R2610 R2613 R2701 R2702 R2705 R2708 R2714 R2716 R2720 R3205 R3301 R3403 R3404 R3405 R3406 R5406 R5407 R5408 R5409 R5410 R5411 R5412 R5413 R5604 R5815 change from 63.R0034.1DL to ZZ.00PAD.M11	change to short pad
X02	10/01	54	del TR5401 TR5402 TR5403 TR5404	delete co-layer
X02	10/01	42	EL4203 change to two ZZ.00PAD.M31	change to short pad
X02	10/01	52	stuff EC5201 EC5202	EMI DMIC noise
X02	10/01	86	stuff SPR2	EMI 1G noise
X02	10/02	56	del R5603 R5602, change net ODD_PWR_5V to 5V_S0	layout spacing
X02	10/02	62	remove KB_BL1 C6202 C6203 F6201 R6210 R6207 R6206 R6208 Q6203	Tulip feature matrix modify
X02	10/03	63	del TR6301 TR6302	delete co-layer
X02	10/03	34	change R3403 R3404 R3405 R3406 from ZZ.00PAD.M11 to 63.R0034.1DL	EMI request
X02	10/06	52	change EC5201 EC5202 from 78.6R864.1FL to 78.22034.1FL (22P)	EMI DMIC noise
X02	10/07	42	add EC4203 EC4204 (78.10422.5FL)	EMI DC_IN power noise
X02	10/07	63	del R6301 R6302 R6303 R6304; add TR6301 TR6302 ( 68.00201.201)	EMI USB2.0 noise
X02	10/08	86	add EC9725 EC9726 EC9727 EC9728 EC9729 (78.10422.5FL)	RF 25M noise
X02	10/08	86	add SPR4 (34.49026.001)	RF 25M noise
A00	10/28	24	change R2424 from 64.47025.6DL (47k) to 64.64925.6DL (64.9k)	PCB Version
A00	10/28	65	change DB1 from 20.D0075.110 to ZZ.00PAD.Y41	Dummy Pad with solder mask
A00	10/28	61	dummy PWRBT1	For X build
A00	10/30	18	dummy R1806 R1813 R1814 R1815	S3 leakage
A00	11/12	63	change CN6301 from 20.K0610.024 to 020.K0139.0024	FAE repair request
A00	11/13	24	change R2408 from ZZ.00PAD.M11 to 63.R0034.1DL & dummy	Synaptics Non PTP request
A00	11/13	62	dummy R6225	Synaptics Non PTP request
A00	11/17	11	add C1145 & dummy it	reserve for 1D05V power

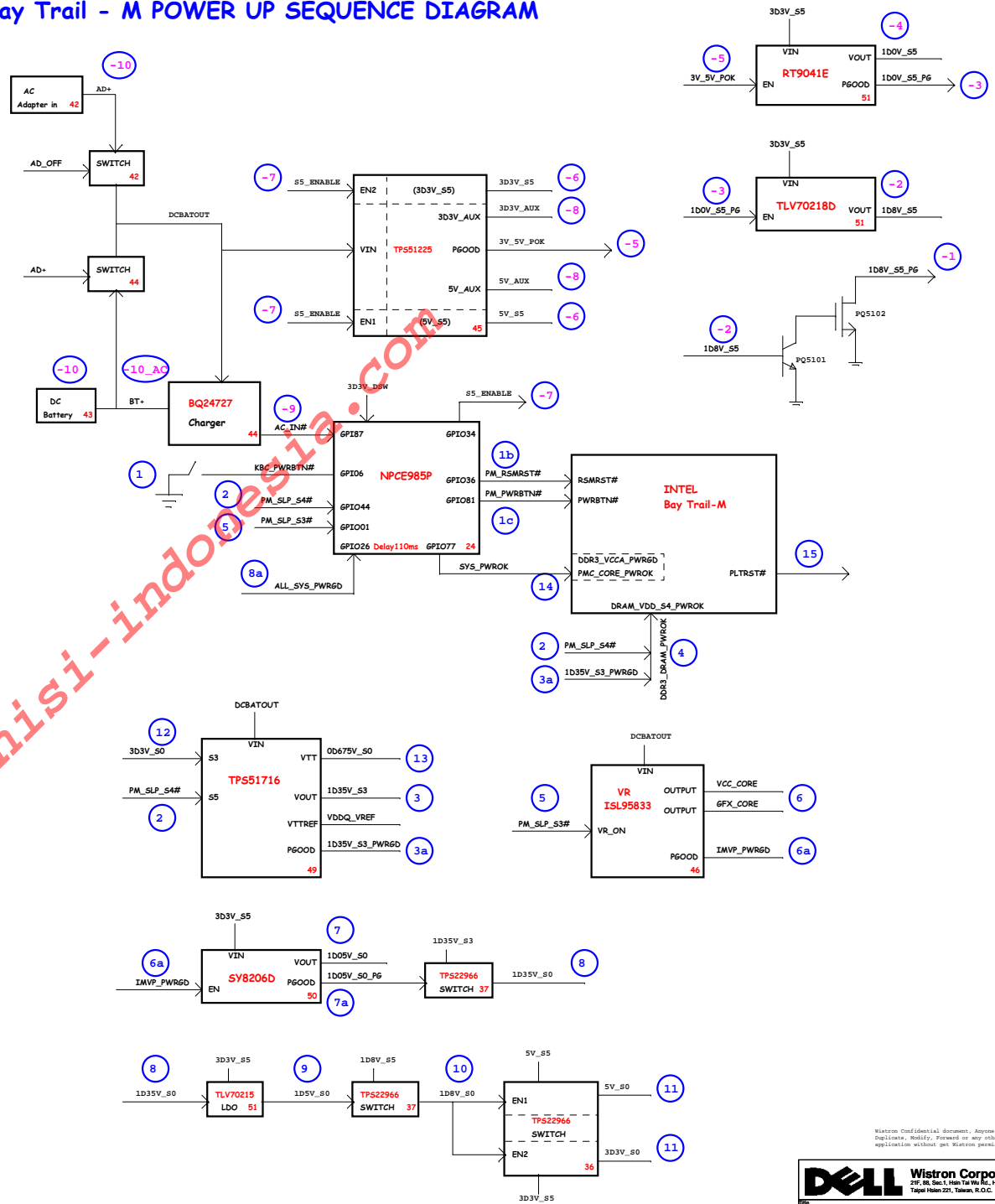
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## Intel-Power Up Sequence with non-S0ix



## Bay Trail - M POWER UP SEQUENCE DIAGRAM

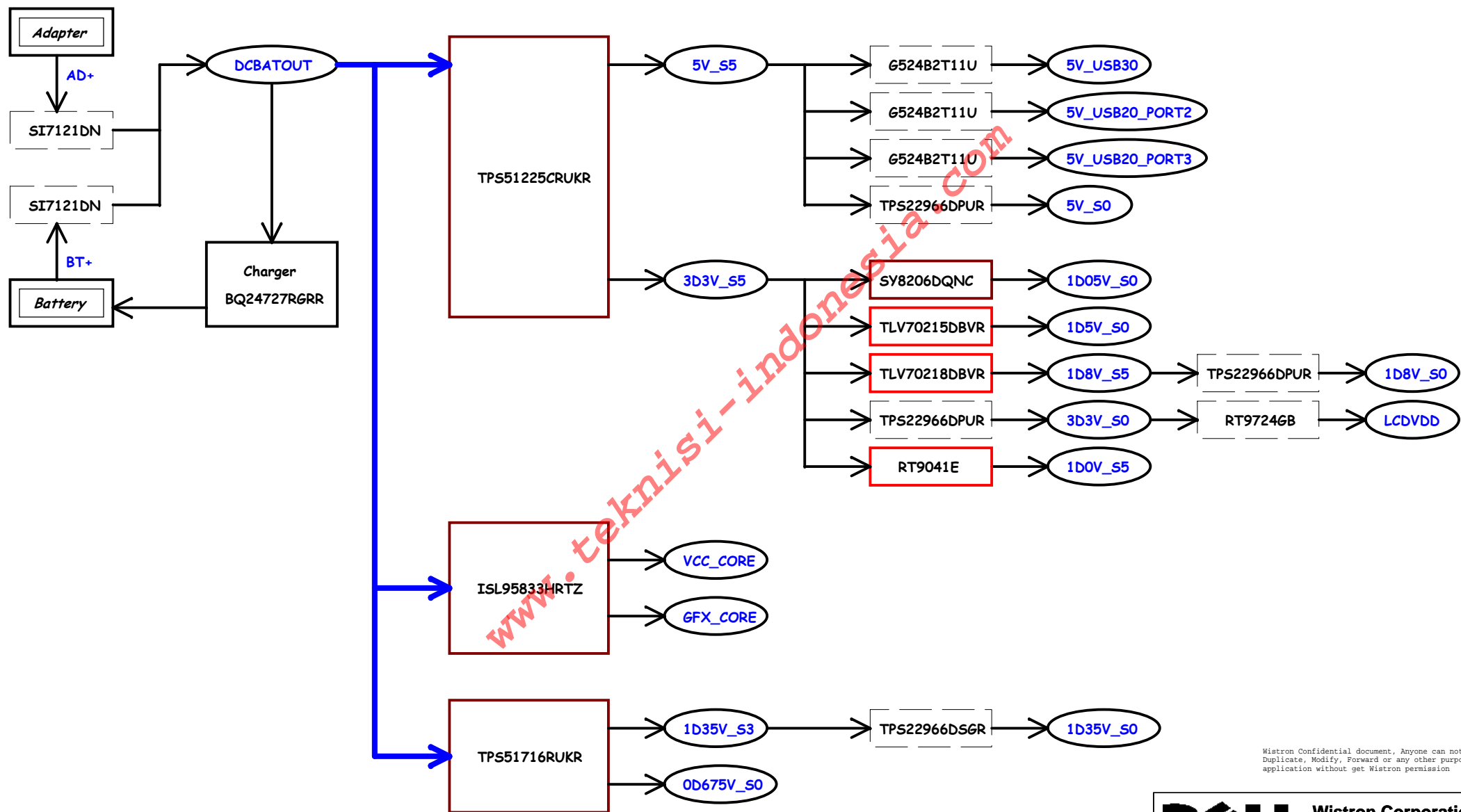


# Power IC Type

Regulator

LDO

Load  
Switch

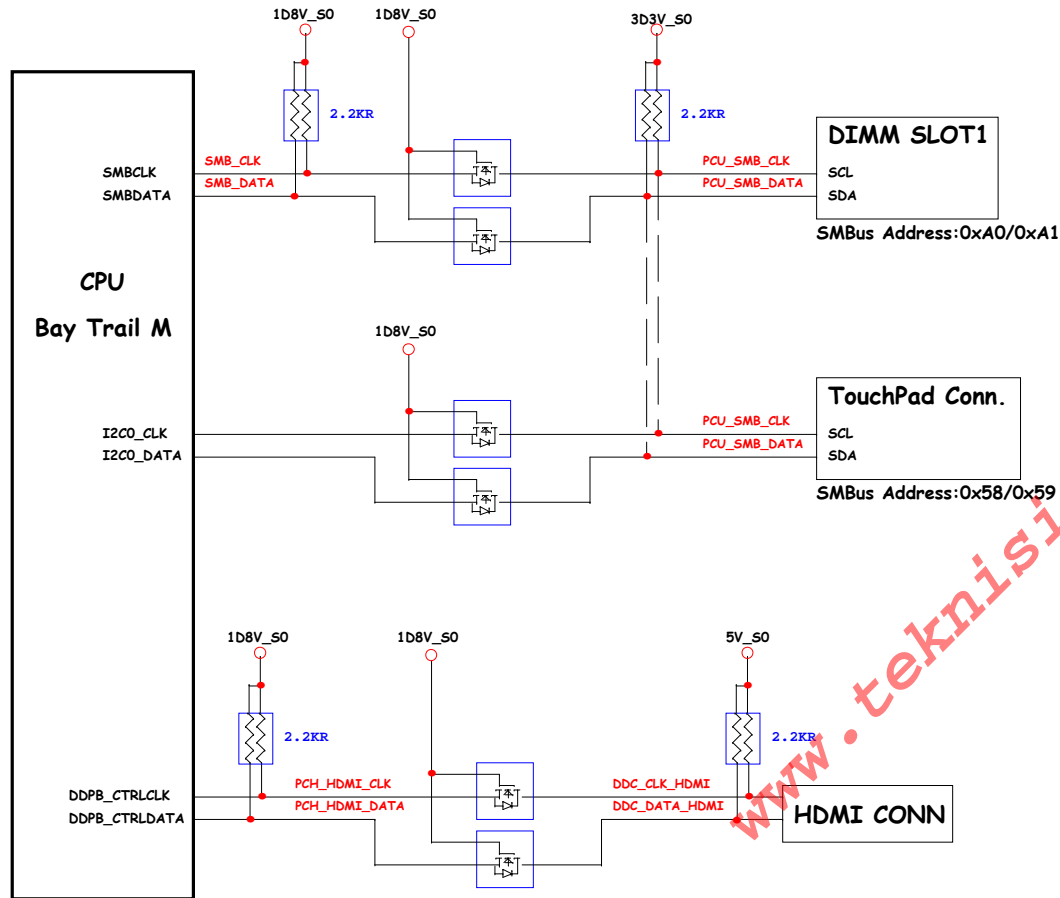


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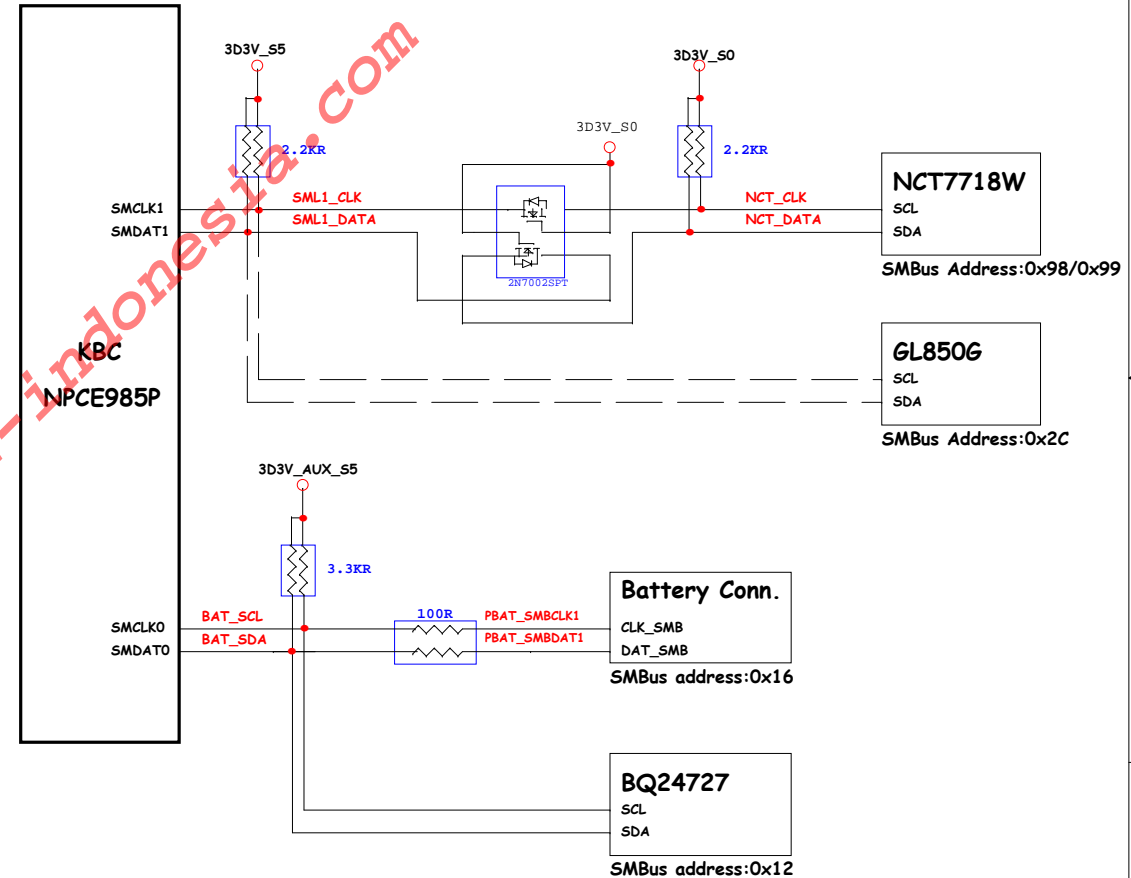
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Power Block Diagram		
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## CPU SMBus / I2C Block Diagram

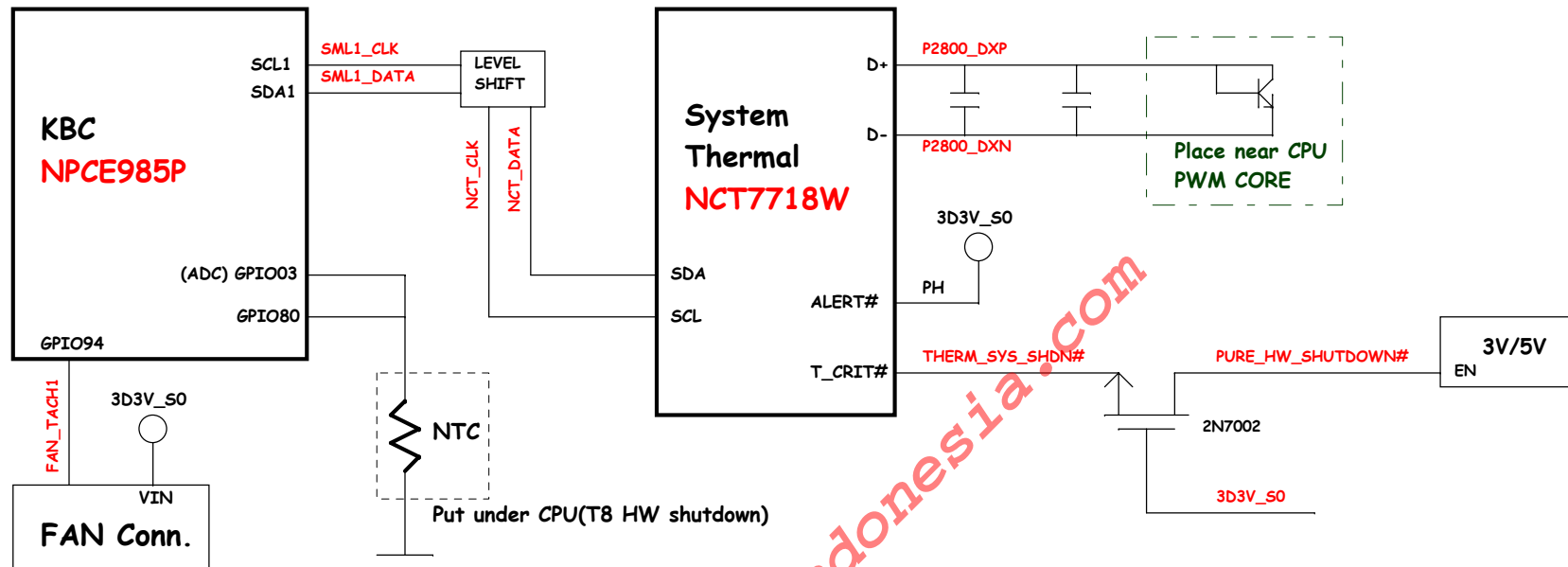


## KBC SMBus Block Diagram

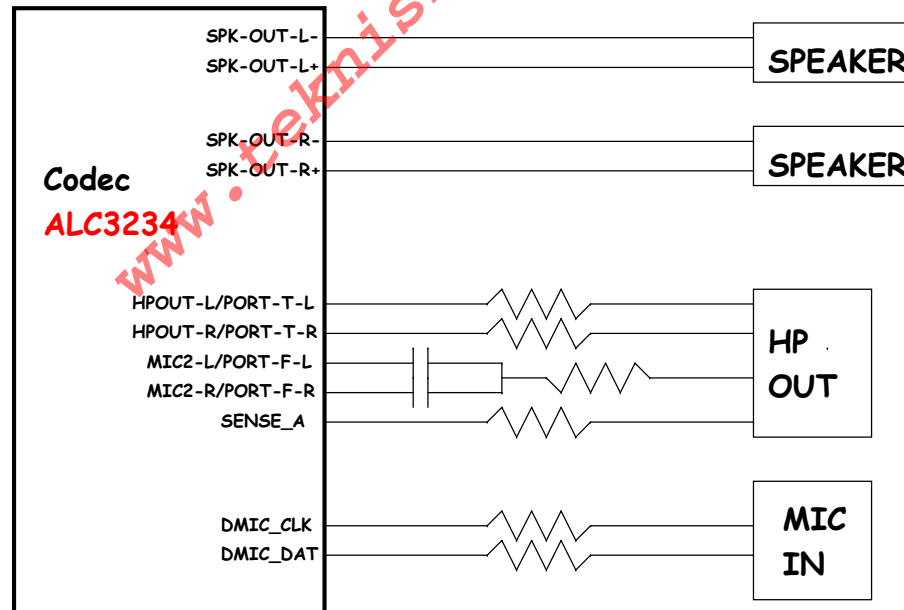


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# Thermal Block Diagram



# Audio Block Diagram



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